



# Cyclone II DSP Development Board

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## Reference Manual



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Document Version: 6.0.1  
Document Date: August 2006

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MNL-C11012805-1.1

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# About This Manual

**Revision History** The table below displays the revision history for the chapters in this manual.

Chapter	Date	Version	Changes Made
All	May 2005	1.0.0	First publication
All	August 2006	6.0.1	Updated for Quartus II Release 6.0 Service Pack 1








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	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
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# Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
<b>Bold Type with Initial Capital Letters</b>	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <b>Save As</b> dialog box.
<b>bold type</b>	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: <b>f<sub>MAX</sub></b> , <b>lqdesigns</b> directory, <b>d:</b> drive, <b>chiptrip.gdf</b> file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: <i>t<sub>PIA</sub></i> , <i>n + 1</i> .  Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <i>&lt;file name&gt;</i> , <i>&lt;project name&gt;.pof</i> file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input . Active-low signals are denoted by suffix n, for example, resetn.  Anything that must be typed exactly as it appears is shown in Courier type (for example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), as well as logic function names (for example, TRI) are shown in Courier.
1., 2., 3., and a., b., c., and so on	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets are used in a list of items when the sequence of the items is not important.
	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

## Introduction

This document describes the hardware features of the Cyclone™ II DSP development board, including detailed pin-out information, to enable designers to create custom FPGA designs that interface with all components on the board.



For information on setting up and powering up the Cyclone II DSP development board and installing the included software, refer to the *DSP Development Kit, Cyclone II Edition Getting Started User Guide*.

## Features Overview

The Cyclone II DSP development board is included in the *DSP Development Kit, Cyclone II Edition* (ordering code DK-DSP-2C70N). The Cyclone II DSP development board provides a low-cost hardware platform for developing high performance DSP designs based on Altera® Cyclone II FPGA devices. The *DSP Development Kit, Cyclone II Edition* features the EP2C70F672 FPGA.

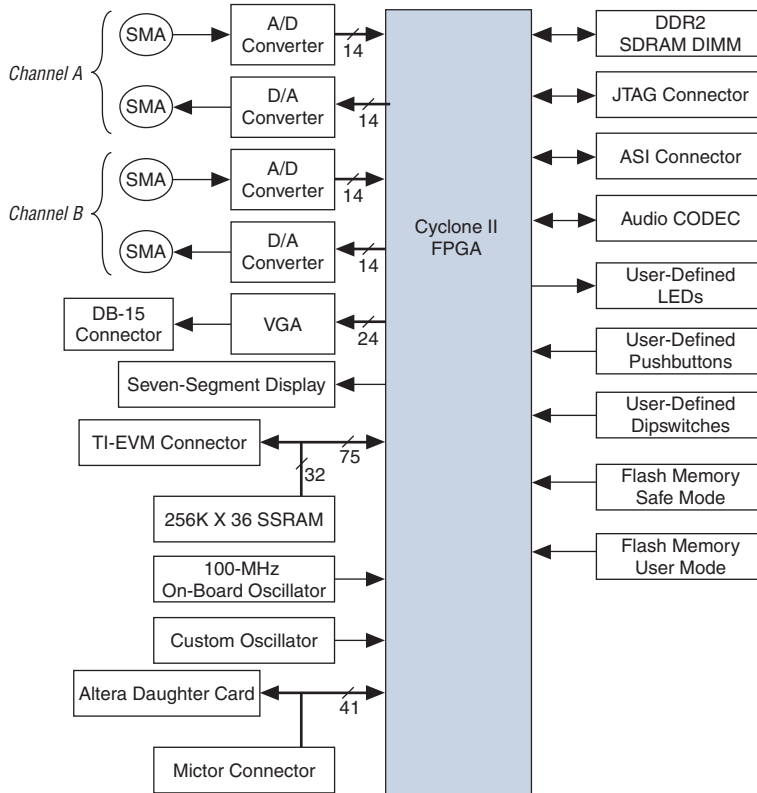
### Components

- Analog I/O
  - Two 14-bit analog-to-digital (A/D) converter channels with 125 MSPS and 70 dB signal-to-noise ratio capabilities
  - Two 14-bit digital-to-analog (D/A) converter channels with 165 MSPS and 70 dB signal-to-noise ratio capabilities
  - One 24-bit RGB VGA adapter with a DB-15 connector
  - One Audio CODEC with input, output, and amplified output
- Memory Subsystem
  - 256 Mbyte DDR2 SDRAM DIMM
  - 1 Mbyte synchronous SRAM (SSRAM)
- Two EPCS64 64 Mbit serial configuration devices
- Debugging Interface—Mictor connector for hardware and software debugging
- Expansion Interfaces
  - 3.3-V/5-V tolerant Altera expansion/prototype headers
  - One Texas Instruments Evaluation Module (TI-EVM) expansion connector to connect to the Spectrum Digital *DSP Starter Kit (DSK) for the TMS320C6416, Revision E*
- Dual seven-segment LED displays
- Eight user-defined LEDs

- One user programmable dual in-line package (DIP) switch (8 positions)
- Four user-defined push-buttons

Figure 1–1 shows a functional diagram of the Cyclone II DSP development board.

**Figure 1–1. Cyclone II DSP Development Board Functional Diagram**





## Introduction

This chapter describes the Cyclone II DSP development board components.

## Components & Interfaces

This section introduces the major components on the Cyclone II DSP development board by first listing them in [Table 2-1 on page 2-4](#). A detailed description of each component comprises the remainder of this chapter.



A schematic, a physical layout database, and manufacturing files for the Cyclone II DSP development board are included in the *DSP Development Kit, Cyclone II Edition* at the following directory:

```
<install-path>\CycloneII_DSP_Kit-v6.0.1\BoardDesignFiles
```



Software and hardware installation and setup are described in the *DSP Development Kit, Cyclone II Edition Getting Started User Guide*.

Figure 2–1 shows the front view of the Cyclone II DSP development board.

**Figure 2–1. Cyclone II DSP Development Board, Front View**

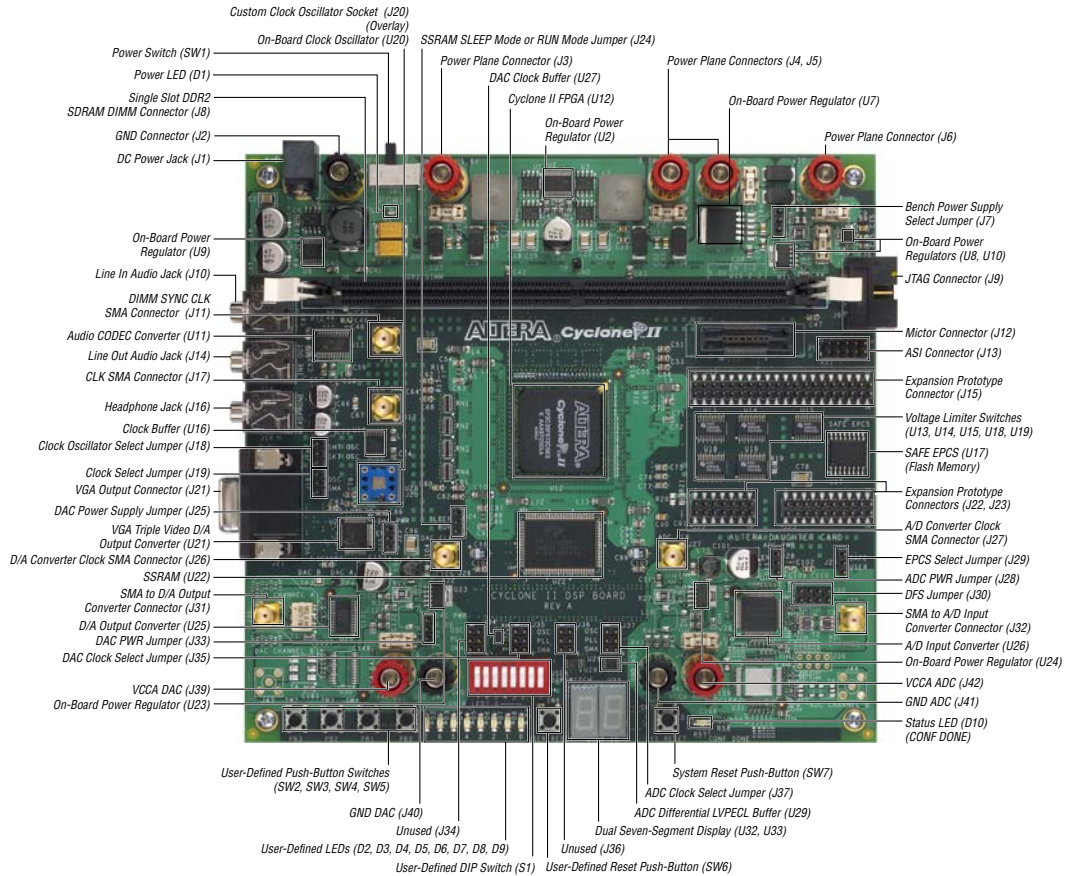
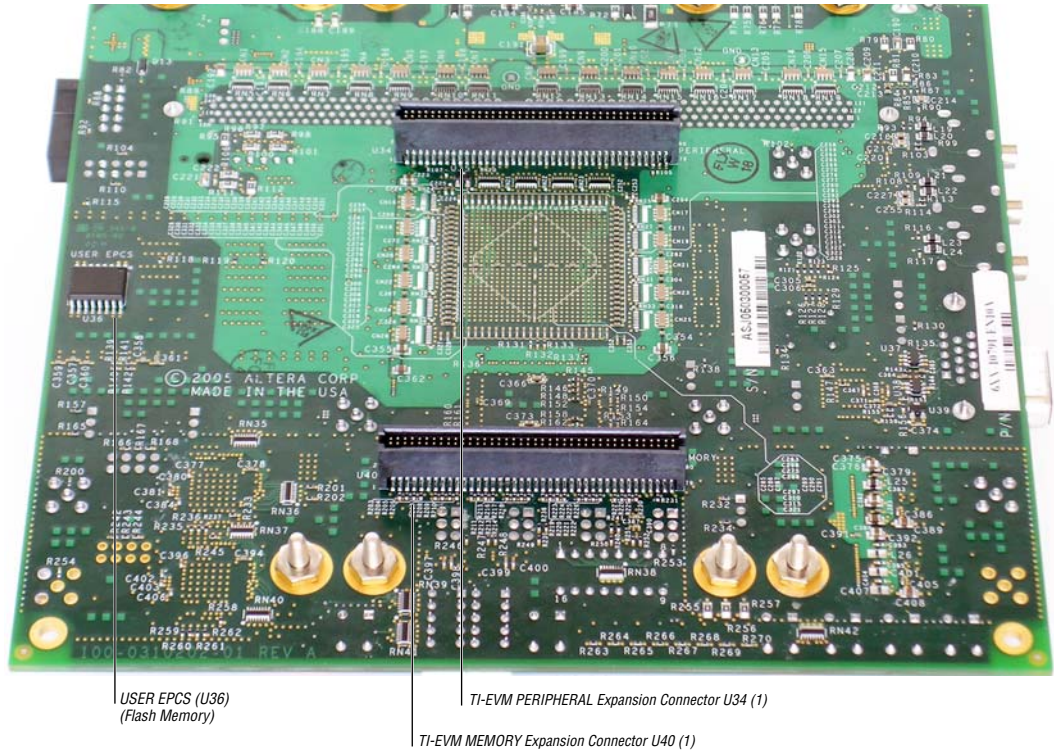


Figure 2-2 shows the back view of the Cyclone II DSP development board.

Figure 2-2. Cyclone II DSP Development Board, Back View



(1) For Spectrum Digital DSP Starter Kit

Table 2–1 describes the major components on the Cyclone II DSP development board and the related interfaces.

<b>Table 2–1. Cyclone II DSP Development Board Components &amp; Interfaces (Part 1 of 5)</b>			
<b>Board Reference</b>	<b>Name</b>	<b>Description</b>	<b>Page</b>
<b>Featured Device</b>			2–9
U12	Cyclone™ II FPGA	EP2C70F672-C6	2–9
<b>User Interfaces</b>			2–9
D2, D3, D4, D5, D6, D7, D8, D9	User-defined LEDs	Eight user-defined LEDs.	2–10
S1	User-defined DIP switch	One User-defined octal DIP switch.	2–11
SW2, SW3, SW4, SW5	User-defined push-button switches	User-defined momentary-contact push-button switches.	2–12
U32, U33	Dual seven-segment display	Dual seven-segment display.	2–13
J10	Line-in audio jack	Audio input connector for line-in (2.5 mm).	2–14
J14	Line-out audio jack	Audio output connector for line-out (2.5 mm).	
J16	Headphone jack	Amplified audio output connector for headphones (2.5 mm).	
U11	Audio CODEC converter	Texas Instruments TLV320AIC23 96 kHz stereo audio CODEC.	2–14
J21	VGA output connector	VGA output connector (DB-15).	2–15
U21	VGA triple video D/A output converter	Fairchild FMS3818 triple video D/A output converter.	2–15
J31 (Channel A) J43 (Channel B)	D/A converter output SMA connector	SMA connector which is driven by the output of the Channel A D/A converter (U25).	2–17
J26 (Channel A & B)	D/A converter CLK SMA connector	SMA connector for an external D/A converter clock input to U25.	2–62
U25 (Channel A) U30 (Channel B)	D/A converter	Texas Instruments DAC904E 14-bit digital-to-analog (D/A) converter.	2–17
J32 (Channel A) J44 (Channel B)	A/D converter input SMA connector	SMA connector which drives the Channel A A/D converter (U26).	2–21
J27 (Channel A & B)	A/D converter CLK SMA connector	SMA connector for an external A/D converter clock input to U26.	2–62
U26 (Channel A) U31 (Channel B)	A/D converter	Texas Instruments ADS5520 12-bit 125 MSPS analog-to-digital (A/D) converter.	2–22

**Table 2–1. Cyclone II DSP Development Board Components & Interfaces (Part 2 of 5)**

Board Reference	Name	Description	Page
<b>Memory Components</b>			<a href="#">2–26</a>
J8	Single slot connector for DDR2 SDRAM DIMM	Micron Technology MT8HTF3264AY-40E, 256 Mbyte, 32 Mbyte x 64, 167 MHz, 1.8 V, 240-pin, non-ECC, unbuffered DDR2 SDRAM DIMM.	<a href="#">2–26</a>
U17, U36	EPCS64 flash memory	Two EPCS64 64 Mbit flash memory, serial configuration devices used to store the safe (factory) design (U17) and a user design (U36). The EPCS64 device configures the EP2C70 FPGA by downloading the factory design or the user design to the EP2C70 FPGA each time the Cyclone II DSP development board powers up or on board reset. J29 determines which design is used.	<a href="#">2–38</a>
U22	SSRAM	Cypress Semiconductor CY7C1360B-166AC, 9 Mbit, 256 Kbit x 36-bit/512 Kbit x 18 pipelined synchronous SRAM (SSRAM).	<a href="#">2–39</a>
		The TMS320C6416 processor memory maps to the Cyclone II DSP development board's SSRAM and the EP2C70 FPGA through the EMIF connector (U34 and U40).	<a href="#">2–42</a>
<b>Expansion Connectors</b>			<a href="#">2–43</a>
J15, J22, J23	Expansion Prototype Connector	Three connectors collectively called the Expansion Prototype Connector. They are used to connect to Altera daughter cards or for debugging and prototyping purposes.	<a href="#">2–43</a>
U34, U40	Expansion TI-EVM connectors	Connects to the EMIF connector on the TMS320C6416 DSK development board. U34 and U40 are located on the back of the Cyclone II DSP development board.	<a href="#">2–47</a>
<b>General Connectors</b>			<a href="#">2–50</a>
J9	JTAG connector	The Joint Test Action Group (JTAG) connector is used to directly configure the EP2C70 FPGA.	<a href="#">2–50</a>
J13	ASI connector	The active serial interface (ASI) connector is used to program the EPCS64.	<a href="#">2–52</a>
J12	Mictor connector	The Mictor connector used for hardware and software debugging. It can be used with external scopes or external logic analyzers.	<a href="#">2–53</a>
J17	CLK SMA connector	SMA connector for an external clock input to U16 to generate FPGA clocks.	<a href="#">2–61</a>

**Table 2–1. Cyclone II DSP Development Board Components & Interfaces (Part 3 of 5)**

Board Reference	Name	Description	Page
J11	DIMM_SYNC_CLK SMA connector	The SMA connector (DIMM_SYNC_CLK) is a test point SMA for eye diagrams of DDR2 signals using AC-coupled SMA connections to an oscilloscope.	2–36
<b>Jumpers</b>			
J18	On-board or custom clock oscillator select jumper	Jumper that determines if the on-board clock 100 MHz oscillator (U20) or a custom clock oscillator (J20) becomes the input clock oscillator to the clock buffer (U16).	2–61
J19	Clock select jumper	Jumper that determines which input to U16 (the selected clock oscillator or the SMA clock) will be used to determine the clock outputs of U16.	2–62
J24	SSRAM SLEEP mode or RUN mode jumper	Jumper that selects SLEEP mode or RUN mode on the SSRAM.	2–37
J7	5 V enable/disable jumper for U10	J7 disables the on-board 5-volt voltage regulator (U10) output to eliminate all regulator-based noise.	2–69
J25	D/A converter power supply jumper	Jumper that selects whether the D/A converter is powered from the DC input jack or the bench power supply connector (J39 and J40).	2–70
J28	A/D converter power supply jumper	Jumper that selects whether the A/D converter is powered from the DC input jack or the bench power supply connector (J42 and J41).	2–70
J33	D/A converter voltage select jumper	Jumper that determines whether the D/A converter is powered at 3.3 volts or 5.0 volts.	2–63
J29	EPCS select jumper	Jumper that selects the configuration mode (SAFE EPCS or USER EPCS)	2–37
J30 (Channel A) J38 (Channel B)	Data Format Select (DFS) jumper	Data Format Select (DFS) jumper selects the data output format from the Texas Instruments ADS5520 A/D converter (U26 and U31). There are four data output formats.	2–21
J35 (Channel A) J34 (Channel B)	D/A converter clock select jumper	D/A Converter Channel A clock select jumper. It determines the D/A converter clock from three input clock signals, the OSC clock, the FPGA D/A converter clock, or the SMA clock (J26).	2–62
J37 (Channel A) J36 (Channel B)	A/D converter clock select jumper	A/D converter Channel A clock select jumper. It determines the A/D converter clock from three input clock signals, the OSC clock, the FPGA A/D converter clock, or the SMA clock (J27).	2–62

**Table 2–1. Cyclone II DSP Development Board Components & Interfaces (Part 4 of 5)**

Board Reference	Name	Description	Page
<b>Status LEDs &amp; Reset/Power Switches</b>			2–57
D1	Power LED	Indicates when power is present.	2–57
D10	Status LED	Indicates successful configuration of the Cyclone II DSP development board (CONFIG_DONE <sub>n</sub> is asserted).	
SW1	Power switch	Power switch that is used to apply power to the on-board power regulators.	2–57
SW6	User-defined reset push-button	USER RESET is user-defined momentary-contact push-button used to reset and initialize a user design on the Cyclone II DSP development board.	2–57
SW7	System reset push-button	SYS RESET is a momentary-contact push-button used to reset the hardware and configure the Cyclone II DSP development board with the design stored in the EPCS64 selected by J29.	2–58
<b>Clocks</b>			2–59
J20	Socket for connecting custom clock oscillator	Socket on top of U20 where a half-can clock oscillator can be installed. It is referred to as the custom clock oscillator. It can be an input to U16.	2–62
U16	Clock buffer	U16 is the clock buffer for the five clocks on the Cyclone II DSP development board.	2–64
U20	On-board clock oscillator	The on-board clock oscillator is the ECS, Inc. ECS-3953M-1000-BN-TR 100 MHz surface mount oscillator. It can be an input to U16.	2–64
U27	D/A converter clock buffer	U27 uses the DAC_A clock selected by J35 and inputs it to U25, and uses the DAC_B clock selected by J34 and inputs it to U30.	2–17
U29	A/D converter differential LVPECL buffer	U29 uses the ADC_A clock selected by J37 and inputs it to U26.	2–22
U28	A/D converter differential LVPECL buffer	U28 uses the ADC_B clock selected by J36 and inputs it to U31.	2–22

**Table 2–1. Cyclone II DSP Development Board Components & Interfaces (Part 5 of 5)**

Board Reference	Name	Description	Page
<b>Power Supply</b>			2–65
J1	DC power jack	9-20 V DC power source. For information on powering up and testing the Cyclone II DSP development board, see “Cyclone II DSP Development Board Power-Up” on page 2–65. For isolating and testing the power planes, see “Bench Power Supplies Using Banana Jacks” on page 2–67.	2–65
U13, U14, U15, U18, U19	Voltage limiter switches	10-bit, 2-port bus switch.	2–66
U2, U7, U8, U9, U10, U23, U24	On-board power regulators	Seven voltage regulators on the Cyclone II DSP development board.	2–66
J2, J3, J4, J5, J6, J39, J40, J41, J42	Power plane connectors	Connectors for bench power supplies.	2–69



## Featured Device

The *DSP Development Kit, Cyclone II Edition* features the EP2C70F672 FPGA (U12) in a 672-pin FineLine BGA® package. [Table 2-2](#) lists the “Power Switch (SW1)” on [page 2-57](#) features of this device.

Feature	Value
Embedded 18x18 multipliers	150
Logic Elements (LEs)	68,416
M4K RAM blocks (4 Kbits + 512 parity bits)	250
Maximum differential channels	262
PLLs	4 PLLs
Total RAM bits	1,152,000
User I/O pins	422

You can configure the FPGA in one of two ways:

- Use Quartus II to program a SRAM Object file (SOF) file directly into the FPGA via the JTAG connector.



For details about configuring the EP2C70 FPGA, see the *Getting Started* chapter in the *DSP Development Kit, Cyclone II Edition Getting Started User Guide*.

- Use Quartus II to load a design into the EPCS64 device via the ASI connector and then cycle power to load the design from the EPCS64 device into the FPGA.

There are two EPCS64 devices, J29 determines which EPCS64 device loads the FPGA. Refer to “[EPCS64 Flash Memory Devices \(U17, U36\)](#)” on [page 2-38](#) for more information.

## User Interfaces

This section describes the user interfaces, which consist of LEDs, switches, push-buttons, seven-segment display, line in, line out, audio and headphone jacks, VGA, D/A converter, and A/D converter.

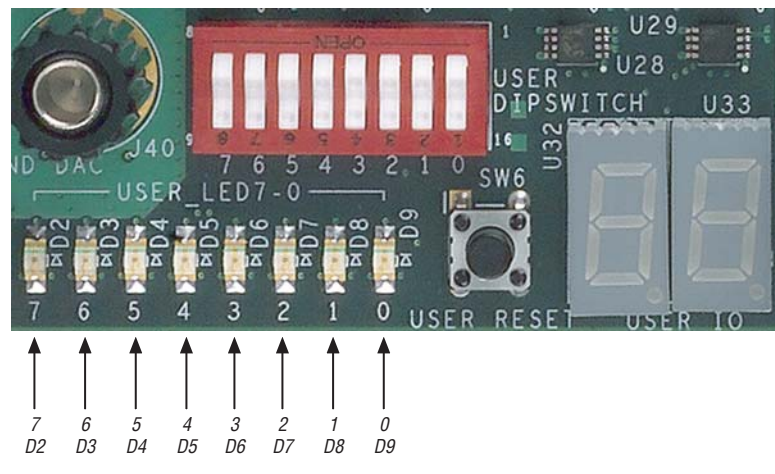
## User-Defined LEDs (D2 Through D9)

The Cyclone II DSP development board provides eight user-defined LEDs. D2 through D9 are connected to general purpose I/O pins on the EP2C70 FPGA as listed in Table 2-3. When the EP2C70 FPGA drives logic 0, the corresponding LED turns on.

LED Number	Board Reference	Schematic Signal Name	Cyclone II (U12) Pin Number
7	D2	USER_LED7	AA7
6	D3	USER_LED6	AA6
5	D4	USER_LED5	AB4
4	D5	USER_LED4	AC3
3	D6	USER_LED3	E22
2	D7	USER_LED2	F20
1	D8	USER_LED1	B3
0	D9	USER_LED0	E5

Figure 2-3 shows the user-defined LEDs.

**Figure 2-3. User-Defined LED0 Through LED7**

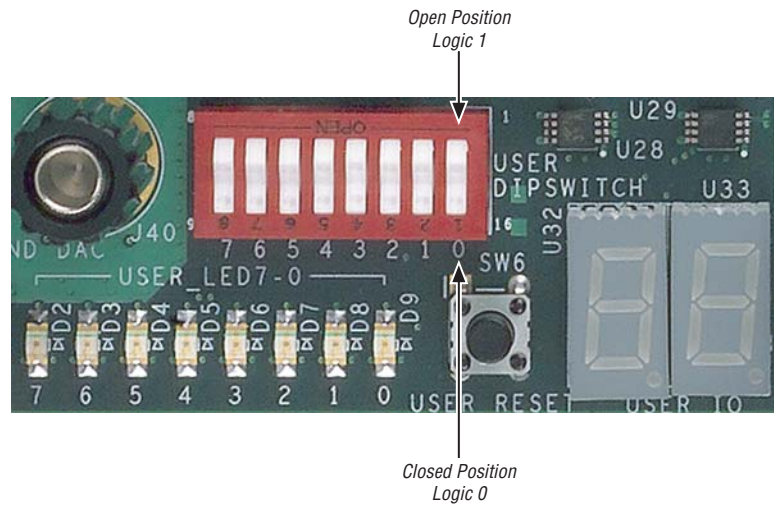


## User Defined DIP Switch (S1)

S1 is a user-defined octal DIP switch available for general-purpose use. It must be defined by the user before it can be used. In the open position, the selected signal is driven to logic 1. In the closed position, the selected signal is driven to logic 0. Table 2-4 lists the pin-outs of the user DIP switch. Figure 2-4 shows the switch labels on the switch, the labels on the printed circuit board (PCB), and shows the open and closed switch positions.

DIP Switch Label	Board Reference	Schematic Signal Name	Cyclone II (U12) Pin Number
1	0	USER_DIPSW0	AC13
2	1	USER_DIPSW1	A19
3	2	USER_DIPSW2	C21
4	3	USER_DIPSW3	C23
5	4	USER_DIPSW4	AF4
6	5	USER_DIPSW5	AC20
7	6	USER_DIPSW6	AE18
8	7	USER_DIPSW7	AE19

**Figure 2-4. User-Defined Dipswitch (S1)**

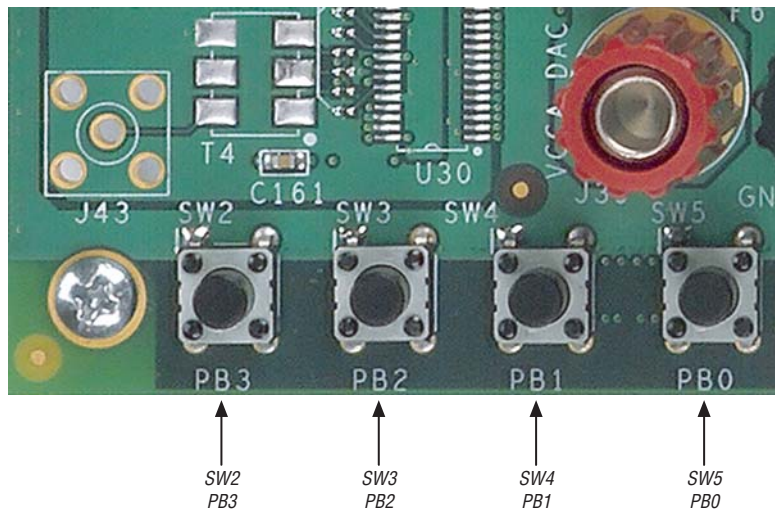


## User-Defined Pushbuttons (SW2 Through SW5)

SW2-SW5 are user-defined momentary-contact push-button switches used to provide stimulus to a user design on the Cyclone II DSP development board. Each push-button is connected to the EP2C70 general-purpose I/O pin as listed in Table 2-5. When the switch is pressed and held down, the device pin is set to logic 0, when the switch is released, the device pin is set to logic 1. Figure 2-5 shows the push-buttons.

Push-Button Name	Board Reference	Schematic Signal Name	Cyclone II (U12) Pin Number
PB3	SW2	USER_PB3	AE14
PB2	SW3	USER_PB2	AE22
PB1	SW4	USER_PB1	AE16
PB0	SW5	USER_PB0	AC18

**Figure 2-5. User-Defined Pushbuttons**

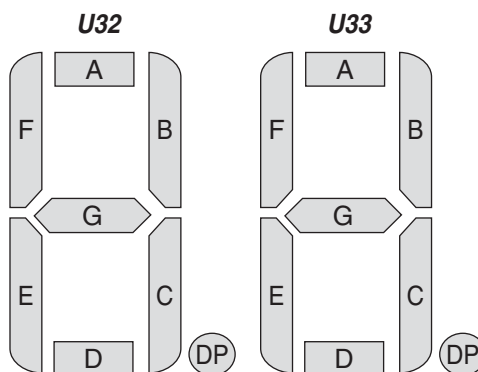


## Seven-Segment Display (U32,U33)

U32 and U33 are dual user defined, seven-segment displays on the Cyclone II DSP development board. Each segment is individually controlled by a general purpose I/O pin. When the EP2C70 FPGA pin drives logic 0, the corresponding segment turns on. Table 2-6 lists the seven-segment display pin-outs. Figure 2-6 shows the name of each segment.

U32			U33		
Segment Display Name	Schematic Signal Name	Cyclone II (U12) Pin Name	Segment Display Name	Schematic Signal Name	Cyclone II (U12) Pin Name
A	DIG_MSB_A	Y21	A	DIG_LSB_A	K2
B	DIG_MSB_B	T7	B	DIG_LSB_B	U25
C	DIG_MSB_C	AB23	C	DIG_LSB_C	AA3
D	DIG_MSB_D	Y5	D	DIG_LSB_D	V1
E	DIG_MSB_E	E1	E	DIG_LSB_E	V7
F	DIG_MSB_F	U1	F	DIG_LSB_F	U23
G	DIG_MSB_G	W21	G	DIG_LSB_G	AC2
DP	DIG_MSB_DP	V3	DP	DIG_LSB_DP	P7

Figure 2-6. Segment Names for the Dual Seven-Segment Displays



## Audio CODEC Converter (U11)

The Cyclone II DSP development board contains three stereo jack connectors, which provide one stereo output, one stereo input, and one amplified stereo headphone output. The stereo jacks are driven by a stereo audio CODEC running at 8-96 kHz. Table 2-7 lists the audio CODEC references.

<i>Table 2-7. Audio CODEC Reference</i>	
Item	Description
Board reference	U11
Part number	TLV320AIC23
Device description	Stereo Audio CODEC, 8-96 kHz
Manufacturer	Texas Instruments
Manufacturer web site	<a href="http://www.ti.com">www.ti.com</a>

Table 2-8 lists the TI TLV320AIC23 audio CODEC pin-outs.

<i>Table 2-8. TI TLV320AIC23 Audio CODEC Pin-Outs</i>		
Schematic Signal Name	Audio CODEC (U11) Pin Number	Cyclone II (U12) Pin Number
AUDIO_BCLK	3	F3
AUDIO_CLK	25	AB3
AUDIO_CSN	21	AC25
AUDIO_DIN	4	J21
AUDIO_DOUT	6	B13
AUDIO_LRCIN	5	W4
AUDIO_LRCOUT	7	AB2
AUDIO_MODE	22	AA2
AUDIO_SCLK	24	R4
AUDIO_SDIN	23	AD2

## Audio Jacks (J10, J14, J16)

The Cyclone II DSP development board contains the following audio connectors:

- J10—an audio connector for line-in
- J14—an audio connector for line-out

- J16—an amplified audio connector output for headphones

These jacks connect to the TI TLV320AIC23 stereo audio CODEC (U11), which controls volume and balance levels and connections. See “[Audio CODEC Converter \(U11\)](#)” on page 2–14.

### VGA Output Connector (J21)

J21 is a standard DB-15 VGA video output connector. This connector interfaces to the Fairchild FMS3818 Triple Video D/A Converter (U21) on the EP2C70 FPGA. J21 allows video images to be displayed on VGA monitors.

### VGA Triple Video D/A Output Converter (U21)

The Cyclone II DSP development board contains a high density DB-15 connector (U21), which outputs VGA and a triple video D/A output converter with the following features:

- 3 x 8 bit, 180 megapixels per second
- $\pm 2.5\%$  gain matching
- $\pm 0.5$  LSB linearity error
- Internal bandgap voltage reference
- Low glitch energy
- One 3.3-V power supply

Table 2–9 lists the VGA triple video D/A output converter device reference.

<b>Item</b>	<b>Description</b>
Board reference	U21
Part number	FMS3818
Device description	Triple Video D/A Converter, 3 x 8 bit, 180 Ms/s
Voltage	3.3 V
Manufacturer	Fairchild Semiconductor
Manufacturer web site	<a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a>

Table 2–10 lists the VGA triple video D/A output converter pin-outs

**Table 2–10. VGA Triple Video D/A Output Converter Pin-Outs (Part 1 of 2) Note (1)**

Schematic Signal Name	VGA (U21) Pin Number	Cyclone II (U12) Pin Number
VGA_B0	16	AC1
VGA_B1	17	W3
VGA_B2	18	B2
VGA_B3	19	W2
VGA_B4	20	H2
VGA_B5	21	W1
VGA_B6	22	U4
VGA_B7	23	U2
VGA_BLANKN	10	U6
VGA_BLUE	29	
VGA_CLK	26	T4
VGA_G0	2	R3
VGA_G1	3	W6
VGA_G2	4	R7
VGA_G3	5	U5
VGA_G4	6	R6
VGA_G5	7	AA4
VGA_G6	8	T6
VGA_G7	9	V4
VGA_GREEN	32	
VGA_HSYNC		H21
VGA_R0	40	Y22
VGA_R1	41	T22
VGA_R2	42	AD25
VGA_R3	43	T20
VGA_R4	44	AC23
VGA_R5	45	U21
VGA_R6	46	P4
VGA_R7	47	Y25



**Table 2–10. VGA Triple Video D/A Output Converter Pin-Outs (Part 2 of 2) Note (1)**

Schematic Signal Name	VGA (U21) Pin Number	Cyclone II (U12) Pin Number
VGA_RED	33	
VGA_SYNCN	11	AE2

**Note to Table 2–10:**

(1) Blank cells indicate no connection.

### D/A Converter SMA Connector (J31 & J43)

J31 (channel A) and J43 (channel B) are standard through-hole SMA connectors used to interface the TI DAC904E D/A converter with SMA cables.

### D/A Converter Clock Buffer (U27 & 30)

For channel A, U27 provides the selected D/A clock to U25. For channel B, U27 provides the selected D/A clock to U30. For more information see “D/A Converter (U25 & U30)” on page 2–17.

### D/A Converter (U25 & U30)

The D/A converter (U25 for channel A and U30 for channel B) on the Cyclone II DSP development board provides 14-bit resolution and produces samples at rates up to 165 MSPS. It is a high-speed TI DAC904E D/A converter and is set up to drive a differential-to-single output through a transformer. The output is transformer coupled and can be found on the SMA connector (J31 for channel A, J43 for channel B). The output of the TI DAC904E D/A converter is set to the maximum output current of 20 mA. The signal-to-noise ratio for the system is 70 dB for output signals from 1 MHz to the Nyquist frequency of the converter.



The SLP-50 anti-aliasing filter from Mini-Circuits provides a 55 MHz cutoff frequency. To use the anti-aliasing filter, connect the filter to one end of the SMA cable. You can perform an external loopback from the SMA D/A converters to the SMA A/D converters using the filter and cable assembly. If the cutoff frequency must be lower than 55 MHz, other filters may be used. See the *Connecting the Cables to the Board & PC* section in the *DSP Development Kit, Cyclone II Edition Getting Started User Guide*.

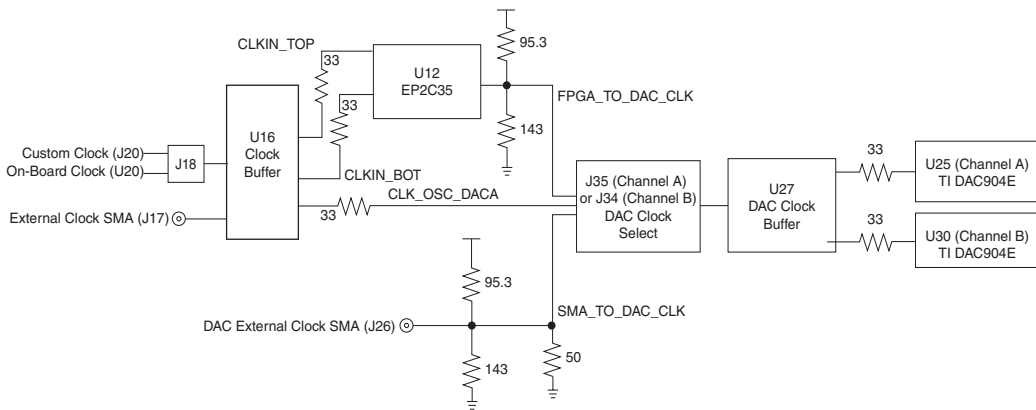
Table 2–11 lists the D/A converter reference for channels A and B.

Item	Description
Board reference	U25 (channel A), U30 (channel B)
Part number	DAC904E
Device description	14-bit 165 MSPS D/A converter
Manufacturer	Texas Instruments
Manufacturer web site	<a href="http://www.ti.com">www.ti.com</a>

### D/A Converter Clocks

Figure 2–7 shows the components involved in selecting the clock signal to be sent to the TI DAC0904E (U25 for channel A, U30 for channel B). J35 (channel A) or J34 (channel B) selects the D/A clock from the OSC clock, the FPGA clock, or the SMA clock (J26). The selected D/A clock passes from J35 through a simple clock buffer (U27), which provides the clock signal to the TI DAC904E.

**Figure 2–7. TI DAC904E D/A Converter Clocking Options**



Refer to “Clock Circuitry” on page 2–59 for information on clock source selection.

Table 2–12 lists the J35 jumper settings used to select the D/A clock.

Clock Source	Board Reference	Schematic Signal Name	D/A Converter Clock Select (J35 & J34) Setting
OSC clock	OSC	CLK_OSC_DACA (Channel A) CLK_OSC_DACB (Channel B)	Pins 1 and 2
FPGA clock	PLL	FPGA_TO_DAC_CLK	Pins 3 and 4
SMA clock (J26)	SMA	SMA_TO_DAC_CLK	Pins 5 and 6

Figure 2–8 shows the J35 and J34 pin-outs listed in Table 2–12. Pins 1 and 2 show an example jumper setting used to select the OSC clock.

**Figure 2–8. J35 & J34 Pin Settings**

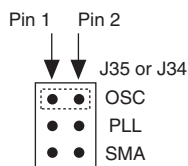


Table 2–13 lists the TI DAC904E D/A converter pin-outs for channel A.

<i>Table 2–13. TI DAC904E D/A Converter Pin-Outs Note (1)</i>		
<b>D/A Converter (U25) Pin Name</b>	<b>D/A Converter (U25) Pin Number</b>	<b>Cyclone II (U12) Pin Number</b>
DAC_A_D0	14	AB1
DAC_A_D1	13	AA1
DAC_A_D2	12	AE3
DAC_A_D3	11	AD3
DAC_A_D4	10	U3
DAC_A_D5	9	T2
DAC_A_D6	8	Y4
DAC_A_D7	7	AA5
DAC_A_D8	6	V5
DAC_A_D9	5	V6
DAC_A_D10	4	P3
DAC_A_D11	3	U7
DAC_A_D12	2	R5
DAC_A_D13	1	P6
DAC_A_IOUTn	21	
DAC_A_IOUTp	22	

**Note to Table 2–13:**

(1) Blank cells indicate no connection.

Table 2–13 lists the TI DAC904E D/A converter pin-outs for channel B.

**Table 2–14. TI DAC904E D/A Converter Pin-Outs** *Note (1)*

D/A Converter (U30) Pin Name	D/A Converter (U25) Pin Number	Cyclone II (U12) Pin Number
DAC_B_D0	14	M4
DAC_B_D1	13	M5
DAC_B_D2	12	U20
DAC_B_D3	11	V20
DAC_B_D4	10	V21
DAC_B_D5	9	B24
DAC_B_D6	8	T23
DAC_B_D7	7	P23
DAC_B_D8	6	Y24
DAC_B_D9	5	V24
DAC_B_D10	4	W25
DAC_B_D11	3	W26
DAC_B_D12	2	V25
DAC_B_D13	1	T25
DAC_B_IOUTn	21	
DAC_B_IOUTp	22	

**Note to Table 2–13:**

(1) Blank cells indicate no connection.

### A/D Converter Data Format Select Jumper (J30 & J38)

The Data Format Select (DFS) jumper is used to select one of four data output formats from the TI ADS5520 A/D converter. Table 2–16 on page 2–22 lists the data output formats and how to select a format with J30 (channel A) or J38 (channel B).

### A/D Converter SMA Connector (J32 & J44)

J32 (channel A) and J44 (channel B) are standard through-hole SMA connectors used to interface the TI ADS5520 A/D input converter with SMA cables.

## A/D Converter Clock Buffer (U29 & U28)

U29 provides the selected A/D clock to U26 for channel A. U28 provides the selected A/D clock to U31 for channel B. For more information, see “A/D Converter (U26 & U31)” on page 2–22.

## A/D Converter (U26 & U31)

The Cyclone II DSP development board contains one TI ADS5520 12-bit 125 MSPS A/D converter. The device is designed for high speed and high-performance applications.

The input to this A/D converter is transformer-coupled in order to create a balanced input. To maximize performance, two transformers (T2, T3) are used in series. The signal-to-noise ratio for the system is 70 dB for input signals from 1 MHz to the Nyquist frequency of the converter. The maximum differential input voltage to the converter is  $2.2 V_{PP}$ .

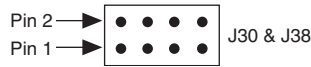
Table 2–15 lists the A/D converter references.

<i>Table 2–15. A/D Converter Reference</i>	
Item	Description
Board reference	U26 (channel A) and U31 (channel B)
Part number	ADS5520
Device description	12-bit 125 MSPS A/D converter
Manufacturer	Texas Instruments
Manufacturer web site	<a href="http://www.ti.com">www.ti.com</a>

The data output format from the A/D converter is selectable through J30 (channel A) or J38 (channel B). Table 2–16 lists the available data output format options and how to set them. Figure 2–9 shows the pin settings for J30 and J38.

<i>Table 2–16. TI ADS5520 A/D Converter (J26) Data Output Format Select</i>		
Jumper (J30 & J38) Setting	Data Format	Clock Output Polarity
Pins 1 and 2	Two's Complement	Data valid on falling edge
Pins 3 and 4	Straight Binary	Data valid on falling edge
Pins 5 and 6	Two's Complement	Data valid on rising edge
Pins 7 and 8	Straight Binary	Data valid on rising edge

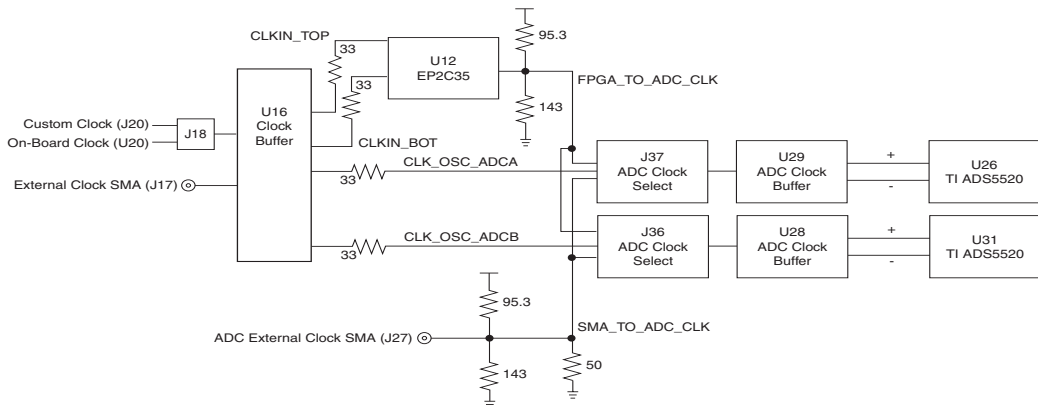
**Figure 2–9. J30 & J38 Pin Settings**



*A/D Converter Clocks*

Figure 2–10 shows the components involved in selecting the clock signal to be sent to the TI ADS5520 A/D converter (U26 for channel A, U31 for channel B). J37 (channel A) or J36 (channel B) selects the A/D clock from the OSC clock, the FPGA clock, or the SMA clock (J27). The selected A/D clock passes through a differential LVPECL buffer (U29 for channel A, U28 for channel B), which provides the clock signal to the TI ADS5520.

**Figure 2–10. TI ADS5520 A/D Converter Clocking Options**



Refer to *“Clock Circuitry”* on page 2–59 for information on clock source selection.

Table 2–17 lists the J37 (channel A) and J36 (channel B) jumper settings used to select the A/D converter clock.

<b>Clock Source</b>	<b>Board Reference</b>	<b>Schematic Signal Name</b>	<b>A/D Converter Clock Select (J37 or J36) Jumper Setting</b>
OSC clock	OSC	CLK_OSC_ADCA (Channel A) CLK_OSC_ADCB (Channel B)	Pins 1 and 2
FPGA clock	PLL	FPGA_TO_ADC_CLK	Pins 3 and 4
SMA clock (J27)	SMA	SMA_TO_ADC_CLK	Pins 5 and 6

Figure 2–11 shows the J37 and J36 pin-outs listed in Table 2–17. Pins 1 and 2 show an example jumper setting used to select the OSC clock.

**Figure 2–11. J37 & J36 Pin Settings**

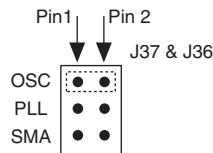




Table 2–18 lists the TI ADS5520 A/D converter pin-outs for channel A.

<b>Table 2–18. TI ADS5520 A/D Converter and EP2C70F672 Pin-Outs</b> <i>Note (1)</i>						
<b>A/D Converter (U26) Pin Name</b>	<b>A/D Converter (U26) Pin Number</b>	<b>Cyclone II (U12) Pin Number</b>		<b>A/D Converter (U26) Pin Name</b>	<b>A/D Converter (U26) Pin Number</b>	<b>Cyclone II (U12) Pin Number</b>
ADC_A_CLK_N	11			ADC_A_D5	52	C11
ADC_A_CLK_P	10			ADC_A_D6	53	B12
ADC_A_CM	17			ADC_A_D7	54	D13
ADC_A_DCLK	43	A13		ADC_A_D8	55	B22
ADC_A_DFS	40			ADC_A_D9	56	A21
ADC_A_INM	20			ADC_A_D10	60	A23
ADC_A_INP	19			ADC_A_D11	61	B23
ADC_A_IREF	31			ADC_A_D12	62	C22
ADC_A_OE	41	F7		ADC_A_D13	63	A22
ADC_A_OVR	64	D15		ADC_A_REFM	30	
ADC_A_D0	44	C5		ADC_A_REFP	29	
ADC_A_D1	45	C6		ADC_A_SEN	4	B18
ADC_A_D2	46	B7		ADC_RESET	35	T24
ADC_A_D3	47	A8		ADC_SCLK	2	AD24
ADC_A_D4	51	A9		ADC_SDATA	3	Y1

**Note to Table 2–18:**

(1) Blank cells indicate no connection.

Table 2–18 lists the TI ADS5520 A/D converter pin-outs for channel B.

**Table 2–19. TI ADS5520 A/D Converter and EP2C70F672 Pin-Outs** *Note (1)*

A/D Converter (U31) Pin Name	A/D Converter (U31) Pin Number	Cyclone II (U12) Pin Number	A/D Converter (U31) Pin Name	A/D Converter (U31) Pin Number	Cyclone II (U12) Pin Number
ADC_B_CLK_N	11		ADC_B_D5	52	B20
ADC_B_CLK_P	10		ADC_B_D6	53	A20
ADC_B_CM	17		ADC_B_D7	54	B21
ADC_B_DCLK	43	C13	ADC_B_D8	55	F18
ADC_B_DFS	40		ADC_B_D9	56	G18
ADC_B_INM	20		ADC_B_D10	60	E18
ADC_B_INP	19		ADC_B_D11	61	F20
ADC_B_IREF	31		ADC_B_D12	62	D21
ADC_B_OE	41	R2	ADC_B_D13	63	D20
ADC_B_OVR	64	A6	ADC_B_REFM	30	
ADC_B_D0	44	F17	ADC_B_REFP	29	
ADC_B_D1	45	D17	ADC_B_SEN	4	D19
ADC_B_D2	46	D18	ADC_RESET	35	T24
ADC_B_D3	47	C19	ADC_SCLK	2	AD24
ADC_B_D4	51	B19	ADC_SDATA	3	Y1

*Note to Table 2–18:*

(1) Blank cells indicate no connection.

## Memory Components

This section describes the memory components on the Cyclone II DSP development board.

### DDR2 SDRAM DIMM (J8)

The Cyclone II DSP development board contains a single slot connector (J8) for a 240-pin DDR2 DIMM module. It has a 72-bit data interface with a full 16-bit address, a 3-bank interface, and supports single and double-sided passive or registered design DIMMs.

The DDR2 SDRAM DIMM is a 256 Mbyte unbuffered non-ECC device in a x64 configuration.



Cyclone II DSP development board uses x64 configuration. The maximum transfer rate of this DIMM is 333 Mbps. The total is  $333 \text{ Mbps} \times 8 = 2,664 \text{ Mbps}$ .

For information about the pin-outs between the Altera DDR2 Controller MegaCore® function and the Cyclone II DSP development board, see [Appendix A, DDR2 SDRAM DIMM Connector Pin Out Table](#).

Table 2–20 lists the DDR2 SDRAM DIMM device reference.

<b>Item</b>	<b>Description</b>
Board reference	J8
Part number	MT8HTF3264AY-40E
Device description	256 Mbyte, 32 Mbyte x 64, 167 MHz, 1.8 V, 240-pin, non-ECC, unbuffered DDR2 SDRAM DIMM
Manufacturer	Micron Technology
Manufacturer web site	<a href="http://www.micron.com">www.micron.com</a>

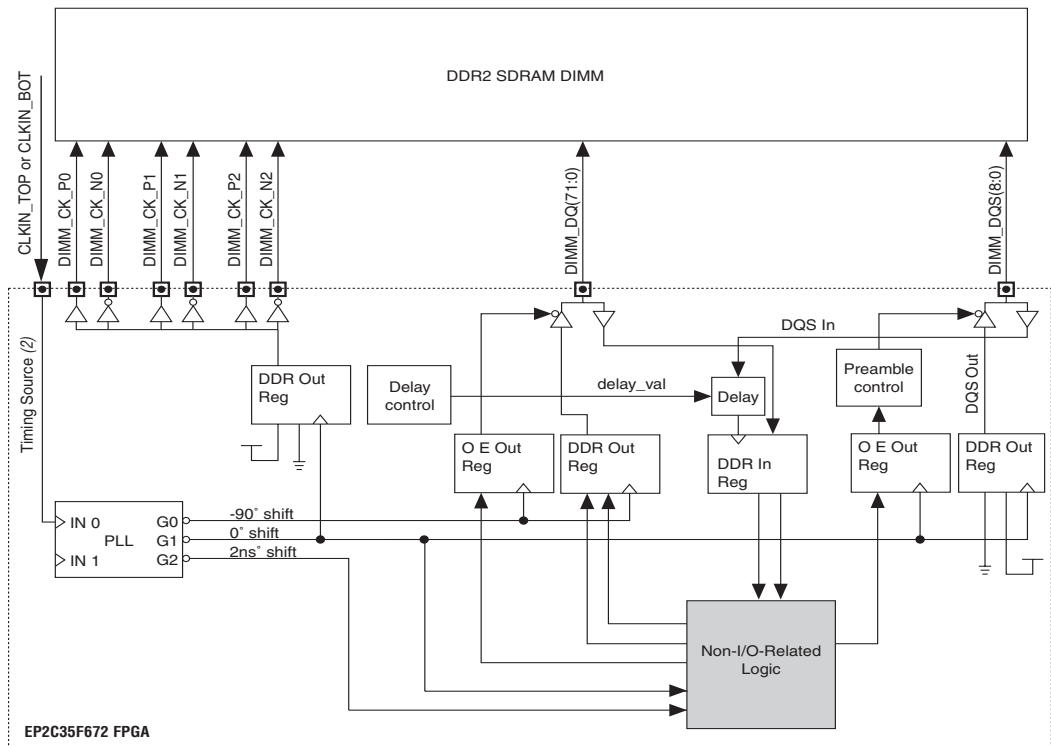
### *DDR2 SDRAM DIMM Clocks*

[Figure 2–12](#) shows the interface to the DDR2 SDRAM DIMM and the required clocking. [Figure 2–12](#) shows the use of the dedicated DDR2 SDRAM DIMM (J8) DQS pins to clock the byte lanes. All clock outputs from the Cyclone II DSP development board use ALTDDIO output registers that can be sourced from any I/O pin. The maximum speed for this interface is 167 MHz.



The J8 connector is Class I terminated.

Figure 2–12. DDR2 SDRAM DIMM Clocking Diagram Note (1)



Note to Figure 2–12:

- (1) One DDR register consists of one I/O register, one core register, and one output multiplexer.
- (2) See Figure 2–21, "Cyclone II DSP Development Board Clocking Options" for timing source information.

Table 2–21 lists the DDR2 SRAM DIMM pin-outs for the EP2C70F672 FPGA.

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 1 of 8) Note (1)**

Cyclone II (U12) Signal Name (2)	DIMM (J8) Signal Name (2)	DIMM (J8) Pin Number	Cyclone II(U12) Pin Number
DIMM_A_R0	DIMM_A0	188	AE4
DIMM_A_R1	DIMM_A1	183	AC8
DIMM_A_R2	DIMM_A2	63	AD6
DIMM_A_R3	DIMM_A3	182	Y10
DIMM_A_R4	DIMM_A4	61	AF5
DIMM_A_R5	DIMM_A5	60	AD7
DIMM_A_R6	DIMM_A6	180	AC6
DIMM_A_R7	DIMM_A7	58	AB8
DIMM_A_R8	DIMM_A8	179	AD5
DIMM_A_R9	DIMM_A9	177	AE11
DIMM_A_R10	DIMM_A10	70	AE5
DIMM_A_R11	DIMM_A11	57	AD4
DIMM_A_R12	DIMM_A12	176	Y12
DIMM_A_R13	DIMM_A13	196	AF7
DIMM_A_R14	DIMM_A14	174	AC5
DIMM_A_R15	DIMM_A15	173	AF13
DIMM_BA_R0	DIMM_BA0	71	Y18
DIMM_BA_R1	DIMM_BA1	190	AF23
DIMM_BA_R2	DIMM_BA2	54	AB15
DIMM_CASN	DIMM_CASN	74	AC22
DIMM_CK_N0	DIMM_CK_N0	186	AD19
DIMM_CK_N1	DIMM_CK_N1	138	AD21
DIMM_CK_N2	DIMM_CK_N2	221	AA20
DIMM_CK_P0	DIMM_CK_P0	185	AC21
DIMM_CK_P1	DIMM_CK_P1	137	AB20
DIMM_CK_P2	DIMM_CK_P2	220	AD22
DIMM_CKE_R0	DIMM_CKE0	52	AE21
DIMM_CKE_R1	DIMM_CKE1	171	AC19
DIMM_CSN_R0	DIMM_CSN0	193	AF22
DIMM_CSN_R1	DIMM_CSN1	76	AB18

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 2 of 8) Note (1)**

<b>Cyclone II (U12) Signal Name (2)</b>	<b>DIMM (J8) Signal Name (2)</b>	<b>DIMM (J8) Pin Number</b>	<b>Cyclone II(U12) Pin Number</b>
DIMM_DM0	DIMM_DM0	125	AC15
DIMM_DM1	DIMM_DM1	134	AA12
DIMM_DM2	DIMM_DM2	146	AC9
DIMM_DM3	DIMM_DM3	155	AD8
DIMM_DM4	DIMM_DM4	202	D6
DIMM_DM5	DIMM_DM5	211	B9
DIMM_DM6	DIMM_DM6	223	G12
DIMM_DM7	DIMM_DM7	232	C16
DIMM_DM8	DIMM_DM8	164	A4
DIMM_DQ0	DIMM_DQ0	3	AA16
DIMM_DQ1	DIMM_DQ1	4	AC17
DIMM_DQ2	DIMM_DQ2	9	AE17
DIMM_DQ3	DIMM_DQ3	10	AF17
DIMM_DQ4	DIMM_DQ4	122	Y16
DIMM_DQ5	DIMM_DQ5	123	AD17
DIMM_DQ6	DIMM_DQ6	128	AF18
DIMM_DQ7	DIMM_DQ7	129	AD16
DIMM_DQ8	DIMM_DQ8	12	Y15
DIMM_DQ9	DIMM_DQ9	13	AA15
DIMM_DQ10	DIMM_DQ10	21	AC14
DIMM_DQ11	DIMM_DQ11	22	AD12
DIMM_DQ12	DIMM_DQ12	131	Y13
DIMM_DQ13	DIMM_DQ13	132	Y14
DIMM_DQ14	DIMM_DQ14	140	AA13
DIMM_DQ15	DIMM_DQ15	141	AE12
DIMM_DQ16	DIMM_DQ16	24	AC11
DIMM_DQ17	DIMM_DQ17	25	AD10
DIMM_DQ18	DIMM_DQ18	30	AE10
DIMM_DQ19	DIMM_DQ19	31	AE9
DIMM_DQ20	DIMM_DQ20	143	AB12
DIMM_DQ21	DIMM_DQ21	144	AD11
DIMM_DQ22	DIMM_DQ22	149	AF10

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 3 of 8) Note (1)**

<b>Cyclone II (U12) Signal Name (2)</b>	<b>DIMM (J8) Signal Name (2)</b>	<b>DIMM (J8) Pin Number</b>	<b>Cyclone II(U12) Pin Number</b>
DIMM_DQ23	DIMM_DQ23	150	AF9
DIMM_DQ24	DIMM_DQ24	33	AB10
DIMM_DQ25	DIMM_DQ25	34	AA10
DIMM_DQ26	DIMM_DQ26	39	AE6
DIMM_DQ27	DIMM_DQ27	40	AE7
DIMM_DQ28	DIMM_DQ28	152	Y11
DIMM_DQ29	DIMM_DQ29	153	AA11
DIMM_DQ30	DIMM_DQ30	158	AF6
DIMM_DQ31	DIMM_DQ31	159	AA9
DIMM_DQ32	DIMM_DQ32	80	F11
DIMM_DQ33	DIMM_DQ33	81	D8
DIMM_DQ34	DIMM_DQ34	86	C8
DIMM_DQ35	DIMM_DQ35	87	D9
DIMM_DQ36	DIMM_DQ36	199	G10
DIMM_DQ37	DIMM_DQ37	200	F10
DIMM_DQ38	DIMM_DQ38	205	A7
DIMM_DQ39	DIMM_DQ39	206	C9
DIMM_DQ40	DIMM_DQ40	89	B10
DIMM_DQ41	DIMM_DQ41	90	A10
DIMM_DQ42	DIMM_DQ42	95	F12
DIMM_DQ43	DIMM_DQ43	96	G11
DIMM_DQ44	DIMM_DQ44	208	D10
DIMM_DQ45	DIMM_DQ45	209	C10
DIMM_DQ46	DIMM_DQ46	214	D12
DIMM_DQ47	DIMM_DQ47	215	E12
DIMM_DQ48	DIMM_DQ48	98	F14
DIMM_DQ49	DIMM_DQ49	99	D14
DIMM_DQ50	DIMM_DQ50	107	B16
DIMM_DQ51	DIMM_DQ51	108	G14
DIMM_DQ52	DIMM_DQ52	217	B11
DIMM_DQ53	DIMM_DQ53	218	G13
DIMM_DQ54	DIMM_DQ54	226	B15

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 4 of 8) Note (1)**

<b>Cyclone II (U12) Signal Name (2)</b>	<b>DIMM (J8) Signal Name (2)</b>	<b>DIMM (J8) Pin Number</b>	<b>Cyclone II(U12) Pin Number</b>
DIMM_DQ55	DIMM_DQ55	227	C15
DIMM_DQ56	DIMM_DQ56	110	A18
DIMM_DQ57	DIMM_DQ57	111	B17
DIMM_DQ58	DIMM_DQ58	116	G16
DIMM_DQ59	DIMM_DQ59	117	G15
DIMM_DQ60	DIMM_DQ60	229	E15
DIMM_DQ61	DIMM_DQ61	230	A17
DIMM_DQ62	DIMM_DQ62	235	F15
DIMM_DQ63	DIMM_DQ63	236	F16
DIMM_DQ64	DIMM_DQ64	42	G9
DIMM_DQ65	DIMM_DQ65	43	C4
DIMM_DQ66	DIMM_DQ66	48	B5
DIMM_DQ67	DIMM_DQ67	49	D7
DIMM_DQ68	DIMM_DQ68	161	F9
DIMM_DQ69	DIMM_DQ69	162	B4
DIMM_DQ70	DIMM_DQ70	167	A5
DIMM_DQ71	DIMM_DQ71	168	C7
DIMM_DQS0	DIMM_DQS0	7	AF19
DIMM_DQS1	DIMM_DQS1	16	AE15
DIMM_DQS2	DIMM_DQS2	28	AE13
DIMM_DQS3	DIMM_DQS3	37	AE8
DIMM_DQS4	DIMM_DQS4	84	B8
DIMM_DQS5	DIMM_DQS5	93	C12
DIMM_DQS6	DIMM_DQS6	105	B14
DIMM_DQS7	DIMM_DQS7	114	C17
DIMM_DQS8	DIMM_DQS8	46	B6
DIMM_ODT_R1	DIMM_ODT1	77	AE23
DIMM_RASN_R	DIMM_RASN	192	AE20
DIMM_WEN_R	DIMM_WEN	73	AA17
	VREF	1	
	1.8V	51	
	1.8V	53	



**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 5 of 8) Note (1)**

Cyclone II (U12) Signal Name (2)	DIMM (J8) Signal Name (2)	DIMM (J8) Pin Number	Cyclone II (U12) Pin Number
	1.8V	56	
	1.8V	59	
	1.8V	62	
	1.8V	64	
	1.8V	67	
	1.8V	69	
	1.8V	72	
	1.8V	75	
	1.8V	78	
	1.8V	170	
	1.8V	172	
	1.8V	175	
	1.8V	178	
	1.8V	181	
	1.8V	184	
	1.8V	187	
	1.8V	189	
	1.8V	191	
	1.8V	194	
	1.8V	197	
	1.8V	238	
	VSS	2	
	VSS	5	
	VSS	8	
	VSS	11	
	VSS	14	
	VSS	17	
	VSS	20	
	VSS	23	
	VSS	26	
	VSS	29	
	VSS	32	

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 6 of 8) Note (1)**

<b>Cyclone II (U12) Signal Name (2)</b>	<b>DIMM (J8) Signal Name (2)</b>	<b>DIMM (J8) Pin Number</b>	<b>Cyclone II(U12) Pin Number</b>
	VSS	35	
	VSS	38	
	VSS	41	
	GND	44	
	GND	47	
	GND	50	
	GND	65	
	GND	66	
	GND	79	
	GND	82	
	GND	85	
	GND	88	
	GND	91	
	GND	94	
	GND	97	
	GND	100	
	GND	103	
	GND	106	
	GND	109	
	GND	112	
	GND	115	
	GND	118	
	GND	121	
	GND	124	
	GND	127	
	GND	130	
	GND	133	
	GND	136	
	GND	139	
	GND	142	
	GND	145	
	GND	148	

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 7 of 8) Note (1)**

Cyclone II (U12) Signal Name (2)	DIMM (J8) Signal Name (2)	DIMM (J8) Pin Number	Cyclone II(U12) Pin Number
	GND	151	
	GND	154	
	GND	157	
	GND	160	
	GND	163	
	GND	166	
	GND	169	
	GND	198	
	GND	201	
	GND	204	
	GND	207	
	GND	210	
	GND	213	
	GND	216	
	GND	219	
	GND	222	
	GND	225	
	GND	228	
	GND	231	
	GND	234	
	GND	237	
	GND	239	
	GND	240	
	GND	101	
		6	
		15	
		19	
		27	
		36	
		45	
		55	
		68	

**Table 2–21. DDR2 SDRAM DIMM Pin-Outs (Part 8 of 8) Note (1)**

Cyclone II (U12) Signal Name (2)	DIMM (J8) Signal Name (2)	DIMM (J8) Pin Number	Cyclone II (U12) Pin Number
		83	
		92	
		102	
		104	
		113	
		126	
		135	
		147	
		156	
		165	
		203	
		212	
		224	

**Notes to Table 2–21:**

- (1) Blank cells indicate no connection.
- (2) In the Cyclone II Signal Name column, some of the names are different than the DIMM (J8) Signal Name due to the use of series resistors.

**DIMM\_SYNC\_CLK SMA Connector (J11)**

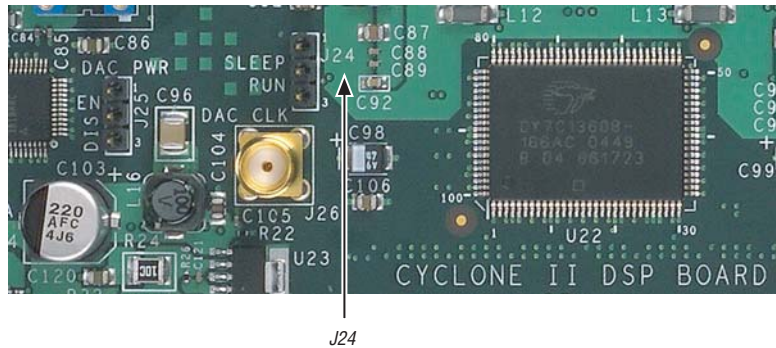
A special feedback clock signal called DIMM\_SYNC\_CLK is included on the board with an SMA(J11) at the end of the trace near its termination point resistor. This signal has two purposes:

- You can use this signal as a test point SMA for eye diagrams of DDR2 signals using AC-coupled SMA connections to an oscilloscope.
- You can use this signal as a board-level round trip delay estimator as an optimal method in resynchronizing DDR2 DIMM read captures with the internal clock (output from the PLL in [Figure 2–12](#)). The length of DIMM\_SYNC\_CLK is the same as the output clocks (.e.g. DIMM\_CK\_PO) and the return clocks (e.g. DIMM\_DQSO).

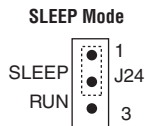
## SSRAM Sleep & Run Modes (J24)

J24 selects SLEEP mode or RUN mode for the SSRAM. A jumper on pins 1 and 2 selects SLEEP mode, a jumper on pins 2 and 3 selects RUN mode, as shown in [Figure 2–13](#) and [Figure 2–14](#).

**Figure 2–13. SSRAM SLEEP & RUN Modes (J24)**



**Figure 2–14. Example of SSRAM in Sleep Mode**



## EPCS Select (J29)

J29 selects the SAFE or USER EPCS configuration mode. See “[EPCS64 Flash Memory Devices \(U17, U36\)](#)” on page 38 for details on how to configure SAFE and USER EPCS configuration modes.

## EPCS64 Flash Memory Devices (U17, U36)

The Cyclone II DSP development board contains two EPCS64 flash memory serial configuration devices (U17, U36) to configure the EP2C70 FPGA using the active serial (AS) configuration scheme.

Use the Quartus II software to program the EPCS64 devices (U17 and U36) via the ASI connector (J13).

- The EPCS64 device labeled U17 (SAFE EPCS) stores the factory design. U17 is preprogrammed with the factory design; you can reprogram U17 using the ASI interface. The EPCS64 device configures the EP2C70 FPGA when J29 has a jumper on pins 1 and 2 and U17 contains valid data.
- The EPCS64 device labeled U36 (USER EPCS) is provided to store a user design. This device configures the EP2C70 FPGA when J29 has a jumper on pins 2 and 3 and U36 contains valid data.



If there is no jumper on J29, the EPCS64 serial configuration devices will not program the EP2C70 FPGA.



The factory design in U17 may be overwritten. If this happens, you can restore it as described in [“Restoring the Factory Design” on page D-1](#).



For additional information about the EP2C70 FPGA, configuring Cyclone II devices, the AS configuration scheme, and the ASMI, see the following documents:

- *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, & EPCS64) Features* chapter in the *Configuration Handbook*, volume 2
- *Active Serial Interface Data Sheet*
- *Configuring Altera FPGAs* chapter in the *Configuration Handbook*, volume 1
- *Configuring Cyclone II Devices* chapter in the *Configuration Handbook*, volume 1
- *Configuration & Testing* chapter in the *Cyclone II Device Handbook*, volume 2
- *Configuring Cyclone II Devices* chapter of the *Cyclone II Device Handbook*, volume 6

## Synchronous SRAM Device (U22)

U22 is the synchronous SRAM (SSRAM), a Cypress Semiconductor CY7C1360B-166 AC SSRAM device with a speed grade of 166 MHz on the Cyclone II DSP development board. It is a 1 Mbyte pipelined 256 Kbit x 36-bit device in a 100-pin TQFP package.



The Cyclone II DSP development board only supports a 32-bit interface due to pin-out constraints on the EP2C70F672.



Some of the SSRAM signal names were changed to facilitate routing ease, reduce layer count, and improve signal integrity. The method of addressing the SSRAM remains the same, but the signal names from the EP2C70 have been changed and do not necessarily match with the SSRAM chip signal names. For a mapping of these signal names, see [Appendix B, SSRAM Pin-Out Table](#).

[Table 2–22](#) lists the SSRAM device reference.

<i>Table 2–22. SSRAM Device Reference</i>	
<b>Item</b>	<b>Description</b>
Board reference	U22
Part number	CY7C1360B-166AC
Device description	9 Mbit, 256 Kbit x 36-bit/512 Kbit x 18 pipelined SSRAM
Manufacturer	Cypress Semiconductors
Manufacturer web site	<a href="http://www.cypress.com">www.cypress.com</a>

Table 2–23 lists the pin connections between the SSRAM and the Cyclone II pin number.

**Table 2–23. SSRAM Device Pin-Outs (Part 1 of 2) Note (1)**

SSRAM Pin Name	SSRAM (U22) Pin Number	Cyclone II (U12) Pin Number	SSRAM Pin Name	SSRAM (U22) Pin Number	Cyclone II (U12) Pin Number
A0	37	K26	DQC25	3	AB26
A1	36	E24	DQC26	6	AA25
A10	99	D25	DQC27	7	AA26
A11	43	K24	DQC28	8	AA24
A12	44	D23	DQC29	9	Y26
A13	45	J25	DQC30	12	W24
A14	46	C25	DQC31	13	U22
A15	47	G26	DQD16	18	V26
A16	48	C24	DQD17	19	U24
A17	49	E26	DQD18	22	U26
A18	38	E25	DQD19	23	T21
A19	39	F26	DQD20	24	R24
A2	82	L25	DQD21	25	P24
A20	42	GND	DQD22	28	AB24
A3	33	H25	DQD23	29	N23
A4	81	L24	DQPA	51	
A5	35	B25	DQPB	80	
A6	100	E23	DQPC	1	
A7	50	K25	DQPD	30	
A8	34	D26	GW_n	88	
A9	32	J26	MODE	31	
ADSC_n	85	L20	NC_14	14	
ADSP_n	84	N24	NC_16	16	
ADV_n	83	M21	NC_66	66	
BWA_n	93	F23	OE_n	86	AA23
BWB_n	94	M23	VDD	15	
BWC_n	95	F25	VDD	41	
BWD_n	96	M24	VDD	65	
BWE_n	87	V23	VDD	91	



**Table 2–23. SSRAM Device Pin-Outs (Part 2 of 2) Note (1)**

SSRAM Pin Name	SSRAM (U22) Pin Number	Cyclone II (U12) Pin Number	SSRAM Pin Name	SSRAM (U22) Pin Number	Cyclone II (U12) Pin Number
CE1_n	98	J24	VDDQ	4	
CE2	97		VDDQ	11	
CE3_n	92	AE25	VDDQ	20	
CLK	89	R25	VDDQ	27	
DQA0	52	G24	VDDQ	54	
DQA1	53	G23	VDDQ	61	
DQA2	56	H24	VDDQ	70	
DQA3	57	H23	VDDQ	77	
DQA4	58	J23	VSS	17	
DQA5	59	J22	VSS	40	
DQA6	62	K23	VSS	67	
DQA7	63	K22	VSS	90	
DQB10	72	L21	VSSQ	5	
DQB11	73	L19	VSSQ	10	
DQB12	74	M20	VSSQ	21	
DQB13	75	N20	VSSQ	26	
DQB14	78	M19	VSSQ	55	
DQB15	79	V22	VSSQ	60	
DQB8	68	K21	VSSQ	71	
DQB9	69	K19	VSSQ	76	

Note to **Table 2–23**:

(1) Blank cells indicate no connection.

## Memory Mapping to the TMS320C6416 Digital Signal Processor

The Spectrum Digital *DSP Starter Kit (DSK) for the TMS320C6416*, Revision E, featuring the TMS320C6416 digital signal processor, interfaces with the Cyclone II DSP development board. This interface is primarily used to memory map the EP2C70 FPGA to the TMS320C6416 processor address space allowing the Cyclone II DSP development board to be used as an FPGA co-processor.

The SSRAM memory is bussed with connectors U34 and U40 to interface with the TMS320C6416 board. The TMS320C6416 board brings out the TMS320C6416's External Memory Interface Connector (EMIF) memory bus to two corresponding headers that connect to U34 and U40. See ["Expansion TI-EVM Connectors \(U34, U40\)"](#) on page 2–47.

The TMS320C6416 processor memory maps to the Cyclone II DSP development board's SSRAM and EP2C70 FPGA with two chip select signals on the TMS320C6416 processor:

- EVM\_CEn2 selects the SSRAM
- EVM\_CEn3 selects the EP2C70 FPGA



The SSRAM cannot be accessed by the EP2C70 FPGA while the TMS320C6416 board is accessing the SSRAM via the TI-EVM connector.

Because the SSRAM and EP2C70 FPGA device are bussed, there is a single naming convention for the signals on the Cyclone II DSP development board. These signals are named relative to the TMS320C6416 board's EMIF interface. For a mapping of these signal names to signals used on the SSRAM, see [Appendix B, SSRAM Pin-Out Table](#).

## Expansion Connectors

This section describes the expansion connectors on the Cyclone II DSP development board.

### Expansion Prototype Connector (J15, J22 & J23)

J15, J22, and J23 are collectively called the Expansion Prototype Connector, as shown in Figure 2-15. J15 is a 2x20 pin connector, while J22 is a 2x7 pin connector, and J23 is a 2x10 pin connector. These connectors have 100-mil spacing between the pins and can be used for Altera daughter cards or for debugging purposes.

**Figure 2-15. Expansion Prototype Connector - J15, J22, & J23**

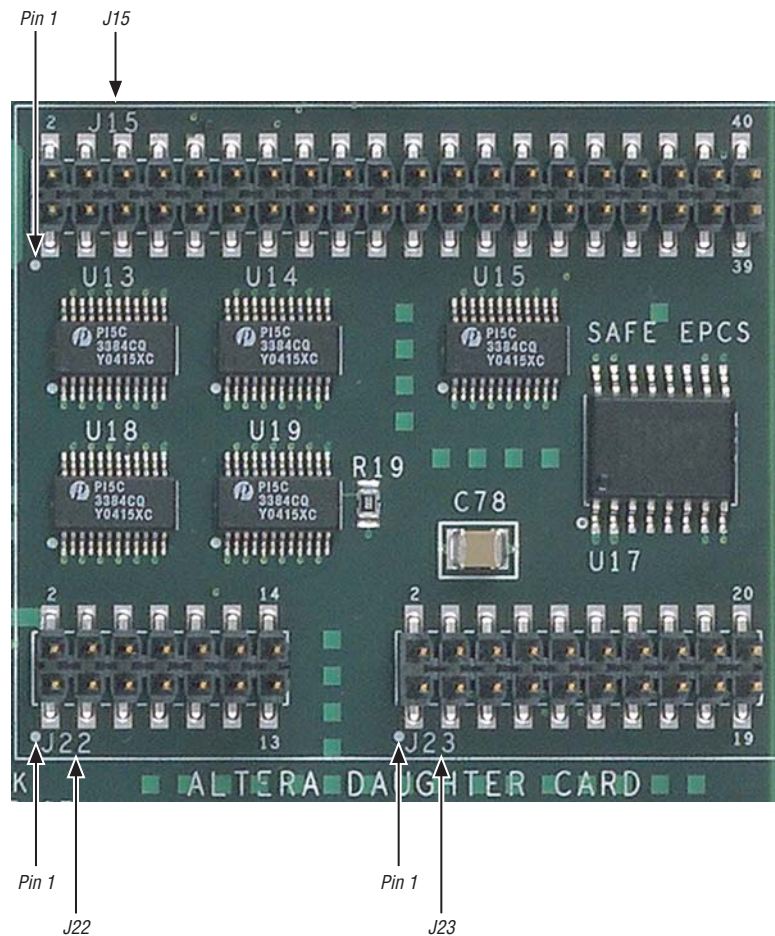
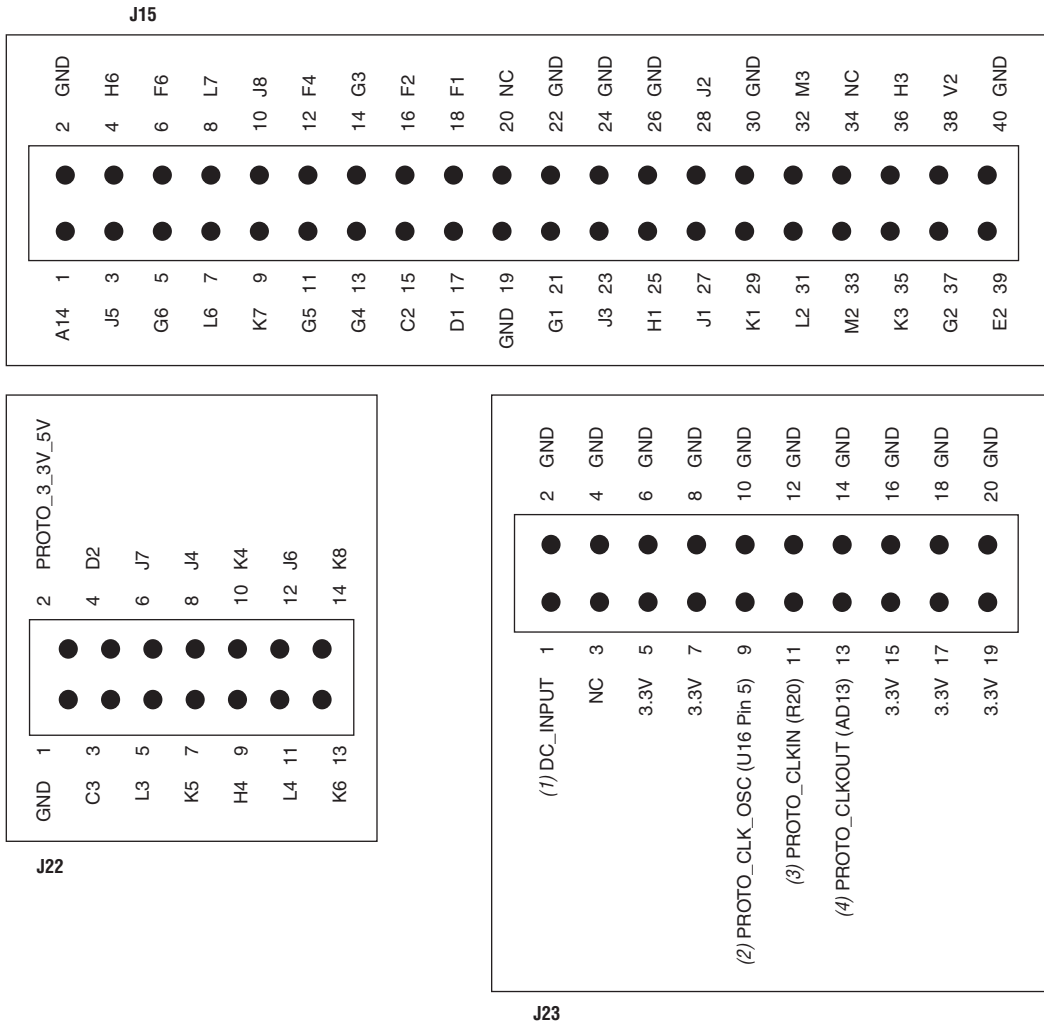


Figure 2–16 shows the Expansion Prototype Connector pin numbers.

Figure 2–16. Expansion Prototype Connector Pin Numbers - J15, J22 & J23



Notes to Figure 2–16:

- (1) Voltage from DC power supply.
- (2) Clock from the clock buffer U16.
- (3) Clock from the EP2C70.
- (4) Clock output from the card connected to the Expansion Prototype Connector.

Table 2–24 lists the Expansion Prototype Connector pin numbers

<b>Table 2–24. Expansion Prototype Connector Pin Numbers - J15, J22 &amp; J23 (Part 1 of 3)</b>			
<b>Cyclone II (U12) Signal Name</b>	<b>Cyclone II (U12) Pin Number</b>	<b>Proto Debug Signal Name</b>	<b>Proto Debug Pin Number (1)</b>
PROTO_IO0	J5	B_PROTO_IO0	J15.3
PROTO_IO1	H6	B_PROTO_IO1	J15.4
PROTO_IO2	G6	B_PROTO_IO2	J15.5
PROTO_IO3	F6	B_PROTO_IO3	J15.6
PROTO_IO4	L6	B_PROTO_IO4	J15.7
PROTO_IO5	L7	B_PROTO_IO5	J15.8
PROTO_IO6	K7	B_PROTO_IO6	J15.9
PROTO_IO7	J8	B_PROTO_IO7	J15.10
PROTO_IO8	G5	B_PROTO_IO8	J15.11
PROTO_IO9	F4	B_PROTO_IO9	J15.12
PROTO_IO10	G4	B_PROTO_IO10	J15.13
PROTO_IO11	G3	B_PROTO_IO11	J15.14
PROTO_IO12	C2	B_PROTO_IO12	J15.15
PROTO_IO13	F2	B_PROTO_IO13	J15.16
PROTO_IO14	D1	B_PROTO_IO14	J15.17
PROTO_IO15	F1	B_PROTO_IO15	J15.18
PROTO_IO16	G1	B_PROTO_IO16	J15.21
PROTO_IO17	J3	B_PROTO_IO17	J15.23
PROTO_IO18	H1	B_PROTO_IO18	J15.25
PROTO_IO19	J1	B_PROTO_IO19	J15.27
PROTO_IO20	J2	B_PROTO_IO20	J15.28
PROTO_IO21	K1	B_PROTO_IO21	J15.29
PROTO_IO22	L2	B_PROTO_IO22	J15.31
PROTO_IO23	M3	B_PROTO_IO23	J15.32
PROTO_IO24	M2	B_PROTO_IO24	J15.33
PROTO_IO25	K3	B_PROTO_IO25	J15.35
PROTO_IO26	H3	B_PROTO_IO26	J15.36
PROTO_IO27	G2	B_PROTO_IO27	J15.37
PROTO_IO28	E2	B_PROTO_IO28	J15.39
PROTO_IO29	D2	B_PROTO_IO29	J22.4
PROTO_IO30	L3	B_PROTO_IO30	J22.5

**Table 2–24. Expansion Prototype Connector Pin Numbers - J15, J22 & J23 (Part 2 of 3)**

Cyclone II (U12) Signal Name	Cyclone II (U12) Pin Number	Proto Debug Signal Name	Proto Debug Pin Number (1)
PROTO_IO31	J7	B_PROTO_IO31	J22.6
PROTO_IO32	K5	B_PROTO_IO32	J22.7
PROTO_IO33	J4	B_PROTO_IO33	J22.8
PROTO_IO34	H4	B_PROTO_IO34	J22.9
PROTO_IO35	K4	B_PROTO_IO35	J22.10
PROTO_IO36	L4	B_PROTO_IO36	J22.11
PROTO_IO37	J6	B_PROTO_IO37	J22.12
PROTO_IO38	K6	B_PROTO_IO38	J22.13
PROTO_IO39	K8	B_PROTO_IO39	J22.14
PROTO_IO40	C3	B_PROTO_IO40	J22.1
		DC_INPUT	J23.1
		3.3V	J23.5
		3.3V	J23.7
		3.3V	J23.15
		3.3V	J23.17
		3.3V	J23.19
		GND	J15.2
		GND	J15.19
		GND	J15.22
		GND	J15.24
		GND	J15.26
		GND	J15.30
		GND	J15.40
		GND	J22.1
		GND	J23.2
		GND	J23.4
		GND	J23.6
		GND	J23.8
		GND	J23.10
		GND	J23.12
		GND	J23.14
		GND	J23.16

**Table 2–24. Expansion Prototype Connector Pin Numbers - J15, J22 & J23 (Part 3 of 3)**

Cyclone II (U12) Signal Name	Cyclone II (U12) Pin Number	Proto Debug Signal Name	Proto Debug Pin Number (1)
		GND	J23.18
		GND	J23.20
		B_PROTO_RESETn	J15.1
	V2	B_PROTO_CARDSELn	J15.38
		PROTO_3_3V_5V	J22.2
		PROTO_CLK_OSC	J23.9
PROTO_CLKIN	R20	PROTO_CLKIN	J23.11
PROTO_CLKOUT	AD13	PROTO_CLKOUT	J23.13

Note to **Table 2–24**:

(1) Unlisted pins have no connection.

## Expansion TI-EVM Connectors (U34, U40)

The TI-EVM connectors connect to the EMIF connectors on the TMS320C6416 board. U34 (labeled PERIPHERAL) and U40 (labeled MEMORY) are located on the back of the Cyclone II DSP development board.

The PERIPHERAL Interface (U34) on the Cyclone II DSP development board connects to the External Peripheral Interface (J3) on the TMS320C6416 board.

The MEMORY Interface (U40) on the Cyclone II DSP development board connects to the External Memory Interface (J4) on the TMS320C6416 board.

Table 2–25 lists the TI-EVM connector pin-outs.

**Table 2–25. TI-EVM Connector Pin-Outs (Part 1 of 4)**

Schematic Signal Name	TI-EVM Connector (U34, U40) Pin Number	Cyclone II (U12) Pin Number
EVM_A10	U40.16	D26
EVM_A11	U40.15	J26
EVM_A12	U40.14	D25
EVM_A13	U40.13	K24
EVM_A14	U40.10	D23

**Table 2–25. TI-EVM Connector Pin-Outs (Part 2 of 4)**

Schematic Signal Name	TI-EVM Connector (U34, U40) Pin Number	Cyclone II (U12) Pin Number
EVM_A15	U40.9	J25
EVM_A16	U40.8	C25
EVM_A17	U40.7	G26
EVM_A18	U40.6	C24
EVM_A19	U40.5	H25
EVM_A2	U40.26	E25
EVM_A20	U40.4	B25
EVM_A21	U40.3	F26
EVM_A3	U40.25	L24
EVM_A4	U40.24	E26
EVM_A5	U40.23	L25
EVM_A6	U40.20	E24
EVM_A7	U40.19	K26
EVM_A8	U40.18	E23
EVM_A9	U40.17	K25
EVM_ARDY	U40.76	W23
EVM_AREN	U40.73	P26
EVM_AWEN	U40.74	V23
EVM_BEN0	U40.30	F23
EVM_BEN1	U40.29	M23
EVM_BEN2	U40.28	F25
EVM_BEN3	U40.27	M24
EVM_CEN2	U40.78	J24
EVM_CEN3	U40.77	AE25
EVM_CLKOUT2	U34.78	P2
EVM_CLKR0	U34.27	G25
EVM_CLKX0	U34.21	F24
EVM_CNTL0	U34.64	M21
EVM_D0	U40.70	V22
EVM_D1	U40.69	AB25
EVM_D10	U40.58	L21
EVM_D11	U40.57	Y26



**Table 2–25. TI-EVM Connector Pin-Outs (Part 3 of 4)**

Schematic Signal Name	TI-EVM Connector (U34, U40) Pin Number	Cyclone II (U12) Pin Number
EVM_D12	U40.56	K19
EVM_D13	U40.55	W24
EVM_D14	U40.54	K21
EVM_D15	U40.53	U22
EVM_D16	U40.50	K22
EVM_D17	U40.49	V26
EVM_D18	U40.48	K23
EVM_D19	U40.47	U24
EVM_D2	U40.68	M19
EVM_D20	U40.46	J22
EVM_D21	U40.45	U26
EVM_D22	U40.44	J23
EVM_D23	U40.43	T21
EVM_D24	U40.40	H23
EVM_D25	U40.39	R24
EVM_D26	U40.38	H24
EVM_D27	U40.37	P24
EVM_D28	U40.36	G23
EVM_D29	U40.35	AB24
EVM_D3	U40.67	AB26
EVM_D30	U40.34	G24
EVM_D31	U40.33	N23
EVM_D4	U40.66	N20
EVM_D5	U40.65	AA25
EVM_D6	U40.64	M20
EVM_D7	U40.63	AA26
EVM_D8	U40.60	L19
EVM_D9	U40.59	AA24
EVM_DMACH0	U34.74	N24
EVM_DR0	U34.30	H26
EVM_DX0	U34.24	G21
EVM_FSR0	U34.29	J20

**Table 2–25. TI-EVM Connector Pin-Outs (Part 4 of 4)**

Schematic Signal Name	TI-EVM Connector (U34, U40) Pin Number	Cyclone II (U12) Pin Number
EVM_FSX0	U34 . 23	G22
EVM_IACK	U34 . 54	N26
EVM_INT0	U34 . 53	M22
EVM_INT1	U34 . 48	M25
EVM_INT2	U34 . 67	AC26
EVM_INT3	U34 . 68	L23
EVM_INUM0	U34 . 58	P1
EVM_OEN	U40 . 75	AA23
EVM_RESET	U34 . 59	P25
EVM_STAT0	U34 . 66	L20

## General Connectors

This section describes the general connectors on the Cyclone II DSP development board.

### JTAG Connector (J9)

The Cyclone II DSP development board contains one JTAG connector (J9). This connector provides communication between a PC running the Quartus II software and the Cyclone II DSP development board. The pins on J9 are connected to J12 through 0- $\Omega$  series resistors, and care must be taken so that signal contention does not occur between the two connectors.

The EP2C70 can be programmed with the JTAG interface. A JTAG UART megafunction is also provided on the *Nios® II Embedded Processor Evaluation Edition, version 6.0.1 CD-ROM* for designers to instantiate in their design as well as a host-side (PC-side) API for transferring data using scripts or compiled programs. You can reach speeds up to 1 Mbps. Nios or Nios II based programmable logic device (PLD) designs can use this interface to control and/or download code.

Table 2–26 lists the JTAG connector pin-outs.

<b>Table 2–26. JTAG Connector Pin-Outs</b>	
<b>Schematic Signal Name</b>	<b>JTAG Connector (J9) Pin Number</b>
JTAG_TCK	1
GND	2
GND	10
3.3V	4
3.3V	6
JTAG_CONN_TDI	3
JTAG_TMS	5
JTAG_CONN_TDO	9

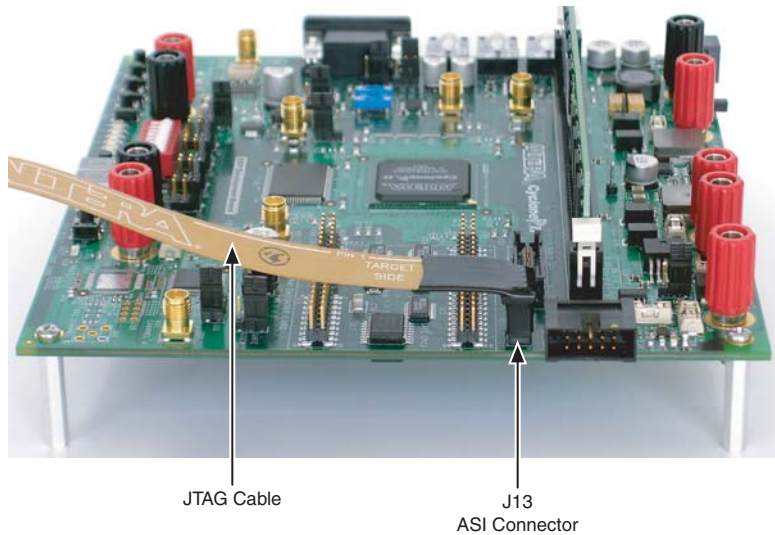
## Active Serial Interface (ASI) Connector (J13)

The active serial interface (ASI) connector is used to program the EPCS64, U17 and U36, using the Quartus II software. See [Figure 2-17](#).

For more information about using J13, see “[EPCS64 Flash Memory Devices \(U17, U36\)](#)” on page 2-38.

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**Figure 2-17. Active Serial Interface Connector With JTAG Cable to Program the EPCS64 Flash Memory**



## Mictor Connector (J12)

The Mictor connector (J12) can be used to transmit up to 27 high-speed I/O signals with very low noise via a shielded Mictor cable. J12 is used as a hardware or software debug port.

Table 2–27 lists the Mictor connector references.

<i>Table 2–27. Mictor Connector Reference</i>	
Item	Description
Board reference	J12
Part number	2-767004-2
Device description	Mictor connector
Manufacturer	AMP
Manufacturer web site	<a href="http://www.amp.com">www.amp.com</a>

The Mictor connector signals are allocated as follows:

- Twenty-five data signals
- One clock input signal
- One clock output signal

Pin allocation is shown in Figure 2–19 on page 2–54 and listed in Table 2–28. Most of the pins on J12 connect to the I/O pins on the EP2C70. For systems that do not use the Mictor connector for debugging the Nios II processor, any on-chip signals can be routed to I/O pins and probed at the Mictor connector (J12) via a Mictor cable.

You can also connect external scopes and logic analyzers to J12 to analyze large number of signals simultaneously.



For details on Nios II debugging products that use the Mictor connector, select the Nios II link on Literature section of the Altera Web site at [www.altera.com](http://www.altera.com).



The JTAG signals have special usage requirements. You cannot use J12 and J9 at the same time.

Figure 2–18 shows the connections from the Mictor connector to the EP2C70 FPGA and the JTAG connector.

**Figure 2–18. Mictor Connector Signaling**

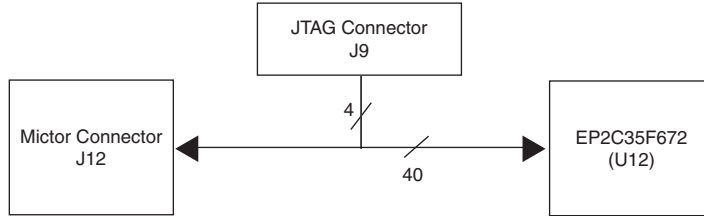
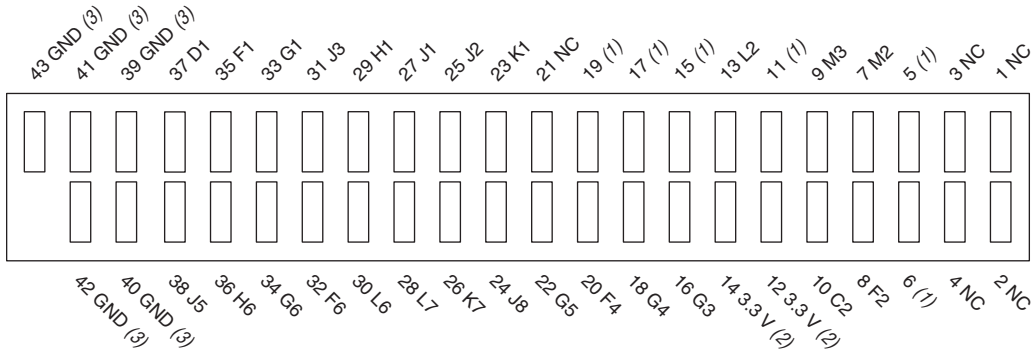


Figure 2–19 shows the J12 pin-outs to the EP2C70. Unless otherwise noted, labels indicate EP2C70 pin numbers.

**Figure 2–19. Mictor Connector (J12) Pin-Outs**



**Notes to Figure 2–19:**

- (1) Pins 5, 6, 11, 15, 17, and 19 are not connected to the EPC335 FPGA.
- (2) Pins 12 and 14 are at 3.3V.
- (3) Pins 39 through 43 are GND.

Table 2–28 lists the Mictor connector pin-outs.

<b>Table 2–28. Table 23 Mictor Connector to Cyclone II Pinout (Part 1 of 2)</b>		
<b>Cyclone II (U12) Pin Number</b>	<b>Mictor (J12) Debug Signal Name</b>	<b>Mictor (J12) Debug Pin Number</b>
J5	PROTO_IO0	38
H6	PROTO_IO1	36
G6	PROTO_IO2	34
F6	PROTO_IO3	32
L6	PROTO_IO4	30
L7	PROTO_IO5	28
K7	PROTO_IO6	26
J8	PROTO_IO7	24
G5	PROTO_IO8	22
F4	PROTO_IO9	20
G4	PROTO_IO10	18
G3	PROTO_IO11	16
C2	PROTO_IO12	10
F2	PROTO_IO13	8
D1	PROTO_IO14	37
F1	PROTO_IO15	35
G1	PROTO_IO16	33
J3	PROTO_IO17	31
H1	PROTO_IO18	29
J1	PROTO_IO19	27
J2	PROTO_IO20	25
K1	PROTO_IO21	80
L2	PROTO_IO22	13
M3	PROTO_IO23	9
M2	PROTO_IO24	7
	GND	39
	GND	40
	GND	41
	GND	42
	GND	43
	3.3V	12

**Table 2–28. Table 23 Mictor Connector to Cyclone II Pinout (Part 2 of 2)**

Cyclone II (U12) Pin Number	Mictor (J12) Debug Signal Name	Mictor (J12) Debug Pin Number
	3.3V	14
	MICTOR_PLDCLK	5
	MICTOR_TR_CLK	6
	MICTOR_TDO	11
	MICTOR_TCK	15
	MICTOR_TMS	17
	MICTOR_TDI	19
	3.3V	12
	3.3V	14

**Note to Table 2–28:**

- (1) Blank cells indicate no connection.



## Status LEDs & Reset/Power Switches

This section describes the status LEDs and reset switches on the Cyclone II DSP development board. Some of the switches are user-defined.

### Power (D1) & Status (D10) LEDs

The power LED (D1) turns on indicating that voltage is supplied to the DC jack, J1, and is being distributed to the Cyclone II DSP development board's on-board power regulators. For information about powering up the Cyclone II DSP development board, see ["Power Switch \(SW1\)" on page 2-57](#).

The Cyclone II DSP development board has one CONF DONE LED (D10) that turns on to indicate successful configuration of the EP2C70 FPGA. This LED is driven by the EP2C70(U12), pin R23 (CONF\_DONE). See [Table 2-29](#).

**Table 2-29. Status & Power LEDs Pin-Outs**

LED Name	Schematic Signal Name	Description
D1	DC_IN	DC Input Power OK
D10	EP2C_CONFIG_DONE	Cyclone II DSP development board successfully configured

### Power Switch (SW1)

SW1 is a power switch that connects the 9-20 V DC input from the DC power jack, J1, to the on-board power regulators. When SW1 is in the ON position, LED (D1) turns on.

### User Defined Reset (SW6) Push-Button

SW6 is a USER RESET momentary-contact push button. It is used as defined by the user, and could be used for initialization and reset of a user design running on the Cyclone II DSP development board. This button must first be defined by the user before it can be used. See [Table 2-30](#).

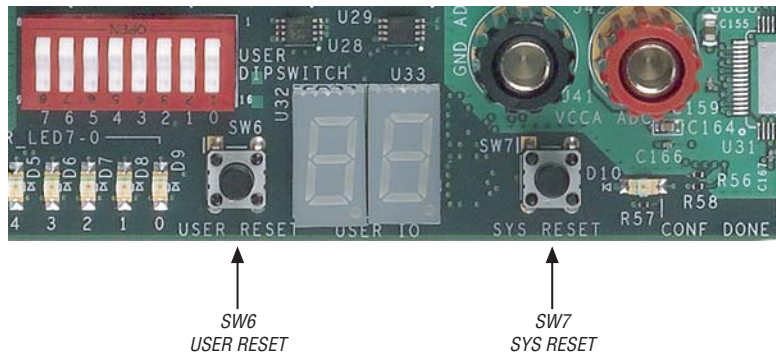
### System Reset (SW7) Push-Button

SW7 is a SYS RESET momentary-contact push button. When pressed, it resets the hardware and programs the EP2C70 FPGA with the design stored in the EPCS64 device. The EPCS64 (U17) device is preprogrammed with the factory design but you can overwrite the factory preprogramming. See [Table 2-30](#).

<i>Table 2-30. SW6 &amp; SW7 Push-Button Pin-Outs</i>		
<b>Push-button</b>	<b>Schematic Signal Name</b>	<b>Cyclone II (U12) Pin Number</b>
SW6 (user-defined)	USER_RESETn	A14
SW7	SYS_RESETn	N7

[Figure 2-20](#) shows the locations of SW6 and SW7.

**Figure 2-20. SW6 USER RESET & SW7 SYS RESET**

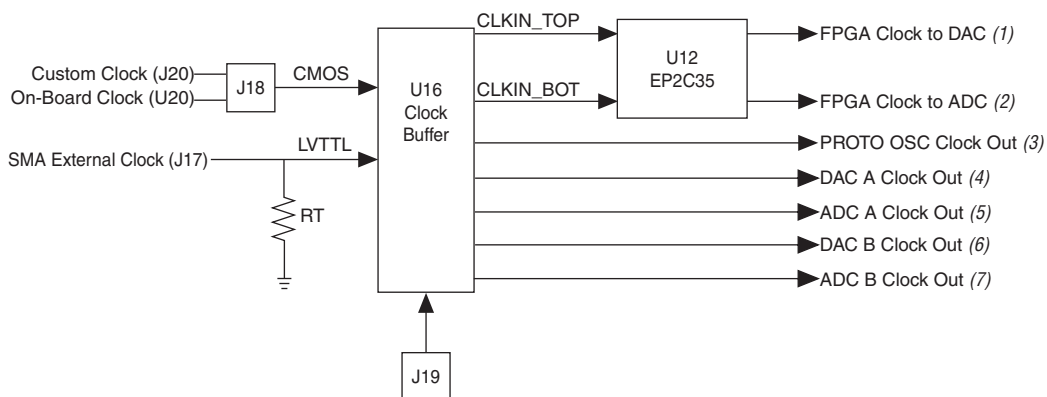


## Clock Circuitry

This section describes the components used to set the Cyclone II DSP development board clocking options.

Figure 2–21 shows the clock distribution on Cyclone II DSP development board. The clocks must be defined first, this occurs within U16, the clock buffer, which generates eight identical clock outputs (one output is unconnected and two outputs are unused) used throughout the Cyclone II DSP development board. See “Clock Buffer (U16)”.

**Figure 2–21. Cyclone II DSP Development Board Clocking Options**



**Notes to Figure 2–21:**

- (1) This signal is input to J35 as the FPGA clock (FPGA\_TO\_DAC\_CLK). See “D/A Converter Clocks” on page 2–18.
- (2) This signal is input to J37 as the FPGA clock (FPGA\_TO\_ADC\_CLK). See “A/D Converter Clocks” on page 2–23.
- (3) This signal is input to J23 as the PROTO clock (PROTO\_CLK\_OSC). See Figure 2–16 on page 2–44.
- (4) This signal is input to J35 as the OSC clock (CLK\_OSC\_DACA). See “D/A Converter Clocks” on page 2–18.
- (5) This signal is input to J37 as the OSC clock (CLK\_OSC\_ADCA). See “A/D Converter Clocks” on page 2–23.
- (6) This signal is input to J34 as the OSC clock (CLK\_OSC\_DACB). See “D/A Converter Clocks” on page 2–18.
- (7) This signal is input to J36 as the OSC clock (CLK\_OSC\_ADCB). See “A/D Converter Clocks” on page 2–23.

## Setting the Clocks

The clocks are selected from one of the following clock sources (as shown in [Figure 2–21](#)):

- The on-board clock oscillator (U20)
- The custom clock oscillator (J20)
- The SMA connector (J17)

The following two jumpers select the clock outputs from the clock buffer (U16). (see [Table 2–31](#)):

1. J18 selects U20 or J20 as the selected clock oscillator to be input to U16.
2. J19 determines which input to U16 (the selected clock oscillator or the SMA clock), will be used to output the clocks.

[Figure 2–22](#) shows U20, the on-board 100 MHz clock oscillator (it is mounted in the gray area as the arrow indicates). If a custom clock oscillator is used, it is installed on the blue socket (J20), as the arrow indicates, on top of U20. [Figure 2–22](#) also shows J18 and J19.

**Figure 2–22. U20/J20, J18 & J19**

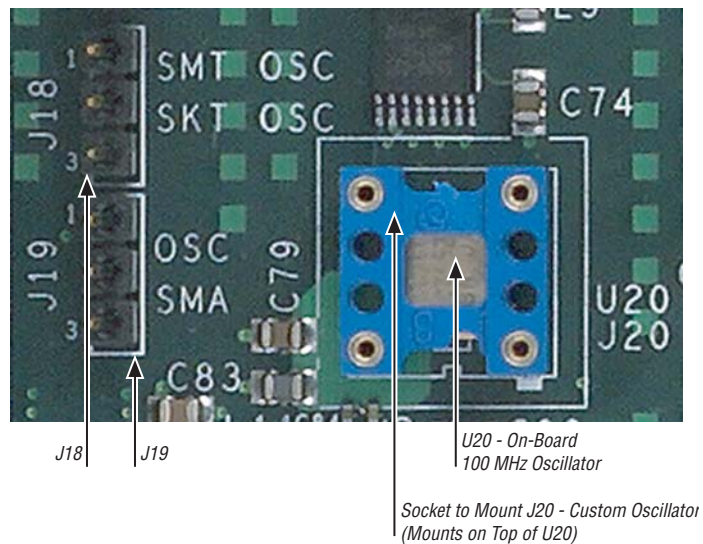


Figure 2–23 shows J18 and J19 with sample jumpers placed on pins 1 and 2. This setting selects the on-board clock oscillator as the input to U16.

**Figure 2–23. J18 & J19 Pin-Outs**

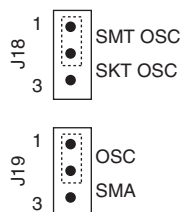


Table 2–31 lists the setting on J18 and J19 that select desired input to be input to U16

Clocking Option	Settings
On-board clock oscillator (U20)	<ul style="list-style-type: none"> <li>On J18, place a jumper on pins 1 and 2.</li> <li>On J19, place a jumper on pins 1 and 2.</li> </ul>
Custom oscillator (J20)	<ul style="list-style-type: none"> <li>Plug a custom half-can oscillator into the J20 socket.</li> <li>On J18, place a jumper on pins 2 and 3.</li> <li>On J19, place a jumper on pins 1 and 2.</li> </ul>
SMA connector (J17)	<ul style="list-style-type: none"> <li>Use J17 (CLK_SMA) for external clock input.</li> <li>On J19, place a jumper on pins 2 and 3.</li> </ul>

### CLK SMA Connector (J17)

The CLK SMA connector (J17) provides an external clock input. It can be selected to be the input to U16. J17 is shown in Figure 2–4 on page 2–11.

An external clock source provides designers, while using a particular design, the flexibility to alter the input frequency to verify  $F_{MAX}$  tolerances.

### On-Board/Custom Clock Oscillators Select Jumper (J18)

J18 selects the on-board clock oscillator (U20) or the custom clock oscillator (J20) as the selected clock oscillator to be input to U16. See Figure 2–22 and Figure 2–23.

## Clock Select Jumper (J19)

J19 determines which input to U16 (the selected clock oscillator or the SMA clock) will be used to determine the clock outputs of U16. See [Figure 2-22](#) and [Figure 2-23](#).

## Socket for a Custom Clock Oscillator (J20)

J20 is a socket for connecting a half-can oscillator that can be used instead of the on-board clock oscillator (U20). An oscillator inserted into J20 is called the custom clock and is not included in the *DSP Development Kit, Cyclone II Edition*. The custom oscillator can be selected to be the input to U16. The J20 socket is mounted on top of U20, the on-board clock oscillator, as shown in [Figure 2-22](#).

## D/A Converter CLK SMA Connector (J26)

J26 is an SMA connector that provides an external clock input to the D/A converter. It can be selected to be the D/A converter clock. See [“D/A Converter Clocks” on page 2-18](#). J26 is shown in [Figure 2-7 on page 2-18](#). [Table 2-12 on page 2-19](#) describes the D/A converter clock source settings.

## A/D Converter CLK SMA Connector (J27)

J27 is an SMA connector that provides an external clock input to the A/D converter. It can be selected to be the A/D clock. See [“A/D Converter Clocks” on page 2-23](#). J27 is shown in [Figure 2-10 on page 2-23](#). [Table 2-17 on page 2-24](#) describes the A/D converter clock source settings.

## D/A Converter CLK Select Jumper (J35 & J34)

J35 is used to choose between three clocking inputs to select the DAC CHANNEL A clock. J34 is used to choose between three clocking inputs to select the DAC CHANNEL B clock. The J35 and J34 D/A converter clock select settings are described in [Table 2-12 on page 2-19](#). J35 and J34 are shown in [Figure 2-7 on page 2-18](#).

## A/D Converter CLK Select Jumper (J37 & J36)

J37 is used to choose between three clocking inputs to select the ADC CHANNEL A clock. J36 is used to choose between three clocking inputs to select the ADC CHANNEL B clock. The J37 and J36 A/D converter clock select settings are described in [Table 2-17 on page 2-24](#). J37 and H36 are shown in [Figure 2-10 on page 2-23](#).

## D/A Converter Power Select Jumper (J33)

J33 determines whether the D/A converter is powered at 3.3 volts or 5 volts. When the jumper is on pins 2 and 3, the D/A converter is powered at 3.3 volts. When the jumper is on pins 1 and 2, the D/A converter is powered at 5 volts.

## Clock Buffer (U16)

U16 generates the clocks used on the Cyclone II DSP development board. U16 generates seven identical clock outputs that carry clock signals to other components on the Cyclone II DSP development board. The clock buffer is a low-skew, single-input to eight-output clock buffer (one output is unconnected and two outputs are unused). [Table 2–32](#) lists the U16 pin-outs.

<b>Clock Buffer Output Pin (U16)</b>	<b>Destination</b>	<b>Description</b>
U16 . 3	U12 . N2	Cyclone II
U16 . 4	U12 . N25	Cyclone II
U16 . 5	J23 . 9	Expansion Prototype Connector
U16 . 11	J37 . 1	A/D converter Channel A Clock Select
U16 . 13	J35 . 1	D/A CONVERTER Channel A Clock Select
U16 . 12	J36 . 1	A/D converter Channel B Clock Select
U16 . 14	J34 . 1	D/A CONVERTER Channel B Clock Select

## On-Board Clock Oscillator (U20)

The on-board clock oscillator is a 100-MHz free-running oscillator that can be used as an input to U16.

Table 2–33 lists the on-board oscillator reference.

<b>Table 2–33. On-Board Oscillator Reference</b>	
<b>Item</b>	<b>Description</b>
Board reference	U20
Part number	ECS-3953M-1000-BN-TR
Device description	100-MHz surface mount oscillator
Manufacturer	ECS, Inc.
Manufacturer web site	<a href="http://www.ecsxtal.com">www.ecsxtal.com</a>

## Power Supply

This section describes the power supply, power regulators, and the power plane connectors.

### DC Power Input Jack (J1)

A 9-20 Volt (V) DC input is provided by a right-angle 2.5 mm power jack with a 5.5mm barrel. Two switching power supplies are used to provide the incoming DC voltage, which is regulated down to 6 V, 3.3 V, and 1.8 V by three switching power supplies. From these voltages all other on-board voltages are generated.

Table 2–34 lists the power-supply specifications.

<b>Table 2–34. Power Supply Specifications</b>	
<b>Item</b>	<b>Description</b>
Board reference	N/A (power supply adapter)
Part number	TR9KT3750LCP-Y
Device description	Switching power supply, Input: 100-240 V, ~1.2 A max., 50-60 Hz Output: +16 V, 3.75 A, 60 W max.
Manufacturer	GlobTek Inc.
Manufacturer web site	<a href="http://www.globtek.com">www.globtek.com</a>



### *Cyclone II DSP Development Board Power-Up*

The Cyclone II DSP development board can be powered up in two ways:

- 9-20 V DC power input jack (J1).
- Bench power supplies (banana jacks), which requires removing fuses to isolate the bench power supplies from the on-board regulators. See [“Bench Power Supplies Using Banana Jacks”](#) on page 2-67.



Before you connect a bench power supply, remove fuses on the Cyclone II DSP development board. All fuses are LITTLEFUSE 154 007 and are 7 A. The fuses do not protect the board from power surges.



For additional information about connecting cables and powering up the Cyclone II DSP development board, see the *Connecting the Cables to the Board and PC* section in the *DSP Development Kit, Cyclone II Edition Getting Started Guide*.

### **Voltage Limiter Switches (U13-U15, U18 & U19)**

Each signal passes through analog switches to protect the EP2C70 from 5-V logic levels. Analog switches are permanently enabled. These voltage limiters combine with J15, J22, and J23, which make up the Expansion Prototype Connector. See [“Expansion Prototype Connector \(J15, J22 & J23\)”](#) on page 2-43 and [“Power Supply”](#) on page 2-65.

## On-Board Power Regulators (U2, U7, U8, U9, U10, U23 & U24)

There are seven voltage regulators on the Cyclone II DSP development board to control eight separate voltage rails. Two switching regulators provide 3.3 V, 1.8 V, and 6 V. Five linear regulators provide 5 V, 1.2 V, 0.9 V, VCCA\_DAC, and VCCA\_ADC. [Table 2–35](#) describes each voltage regulator. See [Figure 2–24](#) for the locations of the voltage regulators on the Cyclone II DSP development board.

**Table 2–35. Cyclone II DSP Development Board Regulators**

Board Reference	Type	Voltage Output	Provides Power To	Manufacturer	Part Number
U2	Dual output switching regulator	3.3 V	<ul style="list-style-type: none"> <li>● Cyclone II VCCIO banks 1, 2, 5, and 6</li> <li>● Clock oscillators and buffers</li> <li>● Expansion Prototype Connector</li> <li>● SSRAM</li> <li>● EPCS64</li> <li>● LEDs and seven-segment displays</li> <li>● DIP switches and push-buttons</li> <li>● Audio CODEC</li> <li>● Video DAC</li> </ul>	Texas Instruments	TPS51020
		1.8 V	<ul style="list-style-type: none"> <li>● DDR2 SDRAM DIMM</li> <li>● Cyclone II VCCIO banks 3, 4, 7, and 8</li> </ul>		TPS51020
U7	Linear regulator	1.2 V	<ul style="list-style-type: none"> <li>● Cyclone II VCCINT</li> <li>● VCCA_PLL</li> <li>● VCCD_PLL</li> </ul>		UC382TD
U8	Linear regulator	0.9 V	<ul style="list-style-type: none"> <li>● DDR2 SDRAM VTT</li> </ul>		TPS51100
U9	Switching regulator	6 V	<ul style="list-style-type: none"> <li>● VCCA_ADC regulator</li> <li>● VCCA_DAC regulator</li> </ul>		TPS40055
U10	Linear regulator	5 V	<ul style="list-style-type: none"> <li>● Linear 0.9V regulator</li> <li>● Expansion Prototype Connector card voltage limiters</li> </ul>		REG104GA
U23	Linear regulator	3.3 V 5 V	<ul style="list-style-type: none"> <li>● D/A Converter voltage</li> </ul>		REG104GA
U24	Linear regulator	3.3 V	<ul style="list-style-type: none"> <li>● A/D Converter voltage</li> </ul>		REG104GA

## Bench Power Supplies Using Banana Jacks

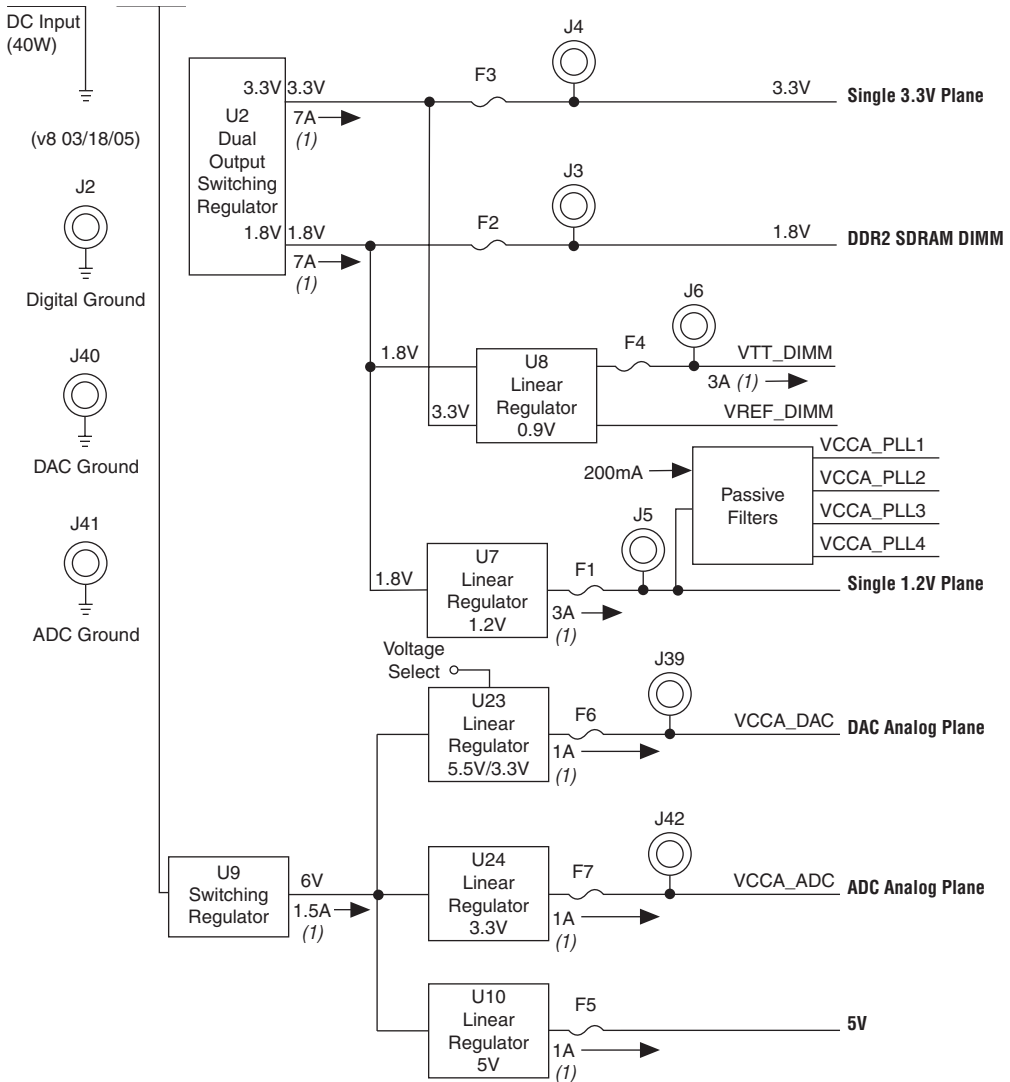
Socketed fuses are provided to isolate the voltage planes from the regulators to allow bench supplies to power these sections using banana jacks. The bench supply inputs are placed after the other power supplies (whether linear or switching supplies) on the Cyclone II DSP development board in order to allow current draw measurements.

Figure 2–24 shows a block diagram of the power supply generation and distribution.



Before you connect a bench power supply, remove fuses on the Cyclone II DSP development board. All fuses are LITTLEFUSE 154 007 and are 7 A. The fuses do not protect the board from power surges.

**Figure 2–24. Cyclone II DSP Development Board Power Distribution Diagram**



(1) Regulators can source up to the indicated current.

## Power Plane Connectors (J2-J6, J39 Through J42)

Bench power supplies provide an easy way to measure the current draw on each power plane. When one plane is being powered by the bench supply, all other planes still draw current from the DC power input. Upon applying power to the Cyclone II DSP development board, the power LED (D1) should be on.

Table 2–36 lists the procedure for powering individual planes through bench power supplies. In the instructions, only remove the fuse listed in the **Settings** column. Other fuses should be left on Cyclone II DSP development board.

<b>Power Plane</b>	<b>Power Plane Using Bench Power Supplies</b>	<b>Settings</b>
3.3V	Cyclone II VCCIO banks 1, 2, 5, and 6, clock oscillators and buffers, Expansion Prototype Connector, SSRAM, EPCS64, LEDs, Audio CODEC, Video DAC, translators	<ul style="list-style-type: none"> <li>● Remove fuse F3</li> <li>● Apply 3.3 V to J4</li> <li>● Apply GND to J2</li> </ul>
1.8V	DDR2 DIMM, Cyclone II VCCIO, banks 3, 4, 7, and 8	<ul style="list-style-type: none"> <li>● Remove fuse F2</li> <li>● Apply 1.8 V to J3</li> <li>● Apply GND to J2</li> </ul>
6V	VCCA_ADC regulator, VCCA_DAC regulator	There is no on-board provision to apply 6 V externally or to remove the regulator from the circuit.
1.2V	Cyclone II VCCINT, VCCA_PLL, and VCCD_PLL	<ul style="list-style-type: none"> <li>● Remove fuse F1</li> <li>● Apply 1.2 V to J5</li> <li>● Apply GND to J2</li> </ul>
5V	Expansion Prototype Connector card voltage limiters	<ul style="list-style-type: none"> <li>● Remove fuse F5</li> <li>● Place a jumper on pins 2 and 3 on J7 to disable the regulator.</li> </ul> <p>There is no on-board provision to apply 5 V externally.</p>
VTT	DDR2 VTT power	<ul style="list-style-type: none"> <li>● Remove fuse F4</li> <li>● Apply 0.9 V to J6</li> <li>● Apply GND to J2</li> </ul>

**Table 2–36. Procedure for Powering Individual Power Planes Through Bench Power Supplies (Part 2 of 2)**

Power Plane	Power Plane Using Bench Power Supplies	Settings
VCCA_ADC	A/D converter power	<ul style="list-style-type: none"> <li>• Remove fuse F7</li> <li>• Place a jumper on pins 2 and 3 on J28 to disable the regulator</li> <li>• Apply 3.3 V to J42</li> <li>• Apply GND to J41</li> </ul>
VCCA_DAC	D/A converter power	<ul style="list-style-type: none"> <li>• Remove fuse F6</li> <li>• Place a jumper on pins 2 and 3 on J25 to disable the regulator</li> <li>• Apply 5 V to J39 and GND to J40</li> </ul> <p>or</p> <ul style="list-style-type: none"> <li>• Apply 3.3 V to J39 and GND to J40</li> </ul>



## Appendix A. DDR2 SDRAM DIMM Connector Pin Out Table

### Introduction

The printed circuit board (PCB) layout for the DDR2 SDRAM DIMM interface to the Cyclone™ II EP2C70 FPGA was optimized for a reduced layer count, reduced via count, and improved signal integrity. This required swapping names from the pin locations created by the DDR2 MegaCore® function's placement and pin-out tool command language (Tcl) script. These swaps only occurred within each octal byte lane (for example, DQ0-DQ7). The result is that, for example, a DDR2 SDRAM DIMM FPGA design in the Quartus® II software will have an I/O called DIMM\_DQ0 (data bit 0) but the corresponding net name on the schematic that this logical pin is connected to is called DIMM\_DQ7 (data bit 7). Conversely, the DIMM\_DQ7 bit is driven to net named DIMM\_DQ0. This swapping list is provided in [Table A-1](#).

Use the DDR2 MegaCore function's default pinout script location for the EP2C70F672 interface width and do not re-assign the pins to match the Cyclone II DSP development board's signal names as DQ data pins. Use [Table A-1](#) if you need to track a particular signal to its destination for eye-diagrams or for general debugging purposes.

**Table A-1. Cyclone II EP2C70F672 DSP Development Board to DIMM Pin Changes (Part 1 of 4)**

Signal Name	Original DDR2 Core Location	EP2C70F672 Board Location	Different (Yes/No)
DIMM_DQ0	AD16	AA16	Yes
DIMM_DQ1	AF17	AC17	Yes
DIMM_DQ2	AE17	AE17	No
DIMM_DQ3	AC17	AF17	Yes
DIMM_DQ4	AD17	Y16	Yes
DIMM_DQ5	AA16	AD17	Yes
DIMM_DQ6	Y16	AF18	Yes
DIMM_DQ7	AF18	AD16	Yes
DIMM_DQ8	AD12	Y15	Yes
DIMM_DQ9	AE12	AA15	Yes
DIMM_DQ10	AC14	AC14	No
DIMM_DQ11	AA13	AD12	Yes
DIMM_DQ12	Y13	Y13	No

**Table A–1. Cyclone II EP2C70F672 DSP Development Board to DIMM Pin Changes (Part 2 of 4)**

Signal Name	Original DDR2 Core Location	EP2C70F672 Board Location	Different (Yes/No)
DIMM_DQ13	Y14	Y14	No
DIMM_DQ14	Y15	AA13	Yes
DIMM_DQ15	AA15	AE12	Yes
DIMM_DQ16	AE9	AC11	Yes
DIMM_DQ17	AF9	AD10	Yes
DIMM_DQ18	AD10	AE10	Yes
DIMM_DQ19	AC11	AE9	Yes
DIMM_DQ20	AE10	AB12	Yes
DIMM_DQ21	AF10	AD11	Yes
DIMM_DQ22	AB12	AF10	Yes
DIMM_DQ23	AD11	AF9	Yes
DIMM_DQ24	AE6	AB10	Yes
DIMM_DQ25	AF6	AA10	Yes
DIMM_DQ26	AA9	AE6	Yes
DIMM_DQ27	AA10	AE7	Yes
DIMM_DQ28	AB10	Y11	Yes
DIMM_DQ29	AA11	AA11	No
DIMM_DQ30	Y11	AF6	Yes
DIMM_DQ31	AE7	AA9	Yes
DIMM_DQ32	F11	F11	No
DIMM_DQ33	C9	D8	Yes
DIMM_DQ34	D9	C8	Yes
DIMM_DQ35	G10	D9	Yes
DIMM_DQ36	F10	G10	Yes
DIMM_DQ37	C8	F10	Yes
DIMM_DQ38	D8	A7	Yes
DIMM_DQ39	A7	C9	Yes
DIMM_DQ40	F12	B10	Yes
DIMM_DQ41	D12	A10	Yes
DIMM_DQ42	E12	F12	Yes
DIMM_DQ43	G11	G11	No
DIMM_DQ44	A10	D10	Yes



**Table A–1. Cyclone II EP2C70F672 DSP Development Board to DIMM Pin Changes (Part 3 of 4)**

Signal Name	Original DDR2 Core Location	EP2C70F672 Board Location	Different (Yes/No)
DIMM_DQ45	B10	C10	Yes
DIMM_DQ46	D10	D12	Yes
DIMM_DQ47	C10	E12	Yes
DIMM_DQ48	B16	F14	Yes
DIMM_DQ49	B15	D14	Yes
DIMM_DQ50	C15	B16	Yes
DIMM_DQ51	G13	G14	Yes
DIMM_DQ52	G14	B11	Yes
DIMM_DQ53	F14	G13	Yes
DIMM_DQ54	D14	B15	Yes
DIMM_DQ55	B11	C15	Yes
DIMM_DQ56	A18	A18	No
DIMM_DQ57	G16	B17	Yes
DIMM_DQ58	F16	G16	Yes
DIMM_DQ59	F15	G15	Yes
DIMM_DQ60	G15	E15	Yes
DIMM_DQ61	B17	A17	Yes
DIMM_DQ62	A17	F15	Yes
DIMM_DQ63	E15	F16	Yes
DIMM_DQ64	C7	G9	Yes
DIMM_DQ65	D7	C4	Yes
DIMM_DQ66	F9	B5	Yes
DIMM_DQ67	G9	D7	Yes
DIMM_DQ68	C4	F9	Yes
DIMM_DQ69	B5	B4	Yes
DIMM_DQ70	A5	A5	No
DIMM_DQ71	B4	C7	Yes
DIMM_DQS0	AF19	AF19	No
DIMM_DQS1	AE15	AE15	No
DIMM_DQS2	AE13	AE13	No
DIMM_DQS3	AE8	AE8	No
DIMM_DQS4	B8	B8	No

**Table A-1. Cyclone II EP2C70F672 DSP Development Board to DIMM Pin Changes (Part 4 of 4)**

<b>Signal Name</b>	<b>Original DDR2 Core Location</b>	<b>EP2C70F672 Board Location</b>	<b>Different (Yes/No)</b>
DIMM_DQS5	C12	C12	No
DIMM_DQS6	B14	B14	No
DIMM_DQS7	C17	C17	No
DIMM_DQS8	B6	B6	No

## Introduction

Because the SSRAM component and the TI EVM board's EMIF interface are bussed, there is a mapping between the signal names. The printed circuit board (PCB) signal names connecting the Cyclone™ II EP2C70F672 FPGA designates the EVM naming conventions. Even though both the SSRAM and TI-EVM have address and data busses they do not map directly (for example, EVM\_D0 connects to SRAM\_D15). [Table B-1](#) lists the mapping. Use this table to create designs that directly interface to the SSRAM.

The Cyclone II signal name corresponds to the net name at the EP2C70F672 FPGA. The SRAM signal name is the net name at the SSRAM.



There is a 22-Ω series resistor between the EP2C70F672 pins and the SSRAM device pins. The SSRAM pin name corresponds to the name assigned to the pin in the SSRAM data sheet.



See the *Cypress CY7C1360B 9-Mbit (256K x 36/512K x 18) Pipelined SRAM* on the Cypress Web site at [www.cypress.com](http://www.cypress.com).

<i>Table B-1. Cyclone II to SSRAM Device Signal Changes (Part 1 of 3) (1)</i>			
Cyclone II (U12) Signal Name	SSRAM (U22) Signal Name	SSRAM (U22) Pin	Cyclone II (U12) Pin Name
EVM_A2	SRAM_A2	82	E25
EVM_A3	SRAM_A3	33	L24
EVM_A4	SRAM_A4	81	E26
EVM_A5	SRAM_A5	35	L25
EVM_A6	SRAM_A1	36	E24
EVM_A7	SRAM_A0	37	K26
EVM_A8	SRAM_A18	38	E23
EVM_A9	SRAM_A19	39	K25
EVM_A10	SRAM_A6	100	D26
EVM_A11	SRAM_A11	43	J26
EVM_A12	SRAM_A12	44	D25
EVM_A13	SRAM_A13	45	K24

**Table B–1. Cyclone II to SSRAM Device Signal Changes (Part 2 of 3) (1)**

<b>Cyclone II (U12) Signal Name</b>	<b>SSRAM (U22) Signal Name</b>	<b>SSRAM (U22) Pin</b>	<b>Cyclone II (U12) Pin Name</b>
EVM_A14	SRAM_A14	46	D23
EVM_A15	SRAM_A15	47	J25
EVM_A16	SRAM_A16	48	C25
EVM_A17	SRAM_A17	49	G26
EVM_A18	SRAM_A7	50	C24
EVM_A19	SRAM_A8	34	H25
EVM_A20	SRAM_A9	32	B25
EVM_A21	SRAM_A10	99	F26
EVM_BEn0	SRAM_BEn0	93	F23
EVM_BEn1	SRAM_BEn1	94	M23
EVM_BEn2	SRAM_BEn2	95	F25
EVM_BEn3	SRAM_BEn3	96	M24
EVM_AWEn	SRAM_BWEn	87	V23
EVM_CEn2	SRAM_CEn1	98	J24
EVM_CNTL0	EVM_ADVn	83	M21
EVM_D0	SRAM_D15	79	V22
EVM_D1	SRAM_D24	2	AB25
EVM_D2	SRAM_D14	78	M19
EVM_D3	SRAM_D25	3	AB26
EVM_D4	SRAM_D13	75	N20
EVM_D5	SRAM_D26	6	AA25
EVM_D6	SRAM_D12	74	M20
EVM_D7	SRAM_D27	7	AA26
EVM_D8	SRAM_D11	73	L19
EVM_D9	SRAM_D28	8	AA24
EVM_D10	SRAM_D10	72	L21
EVM_D11	SRAM_D29	9	Y26
EVM_D12	SRAM_D9	69	K19
EVM_D13	SRAM_D30	12	W24
EVM_D14	SRAM_D8	68	K21
EVM_D15	SRAM_D31	13	U22
EVM_D16	SRAM_D7	63	K22

**Table B-1. Cyclone II to SSRAM Device Signal Changes (Part 3 of 3) (1)**

Cyclone II (U12) Signal Name	SSRAM (U22) Signal Name	SSRAM (U22) Pin	Cyclone II (U12) Pin Name
EVM_D17	SRAM_D16	18	V26
EVM_D18	SRAM_D6	62	K23
EVM_D19	SRAM_D17	19	U24
EVM_D20	SRAM_D5	59	J22
EVM_D21	SRAM_D18	22	U26
EVM_D22	SRAM_D4	58	J23
EVM_D23	SRAM_D19	23	T21
EVM_D24	SRAM_D3	57	H23
EVM_D25	SRAM_D20	24	R24
EVM_D26	SRAM_D2	56	H24
EVM_D27	SRAM_D21	25	P24
EVM_D28	SRAM_D1	53	G23
EVM_D29	SRAM_D22	28	AB24
EVM_D30	SRAM_D0	52	G24
EVM_D31	SRAM_D23	29	N23
EVM_DMAC0	EVM_ADSPn	84	N24
EVM_OEn	SRAM_OEn	86	AA23
EVM_STAT0	SRAM_ADSCn	85	L20
GND	SRAM_A20	42	
SRAM_CLK	SRAM_CLK_R	89	R25
	SRAM_CE2	97	
	SRAM_CEn3	92	
	SRAM_DQP0	51	
	SRAM_DQP1	80	
	SRAM_DQP2	1	
	SRAM_DQP3	30	
	SRAM_GWn	88	
	SRAM_MODE	31	

**Note to Table B-1:**

(1) Blank cells indicate no connection.





# Appendix C. Cyclone II EP2C70 Device Pin-Out Table

## Introduction

Table C-1 lists the Cyclone™ II EP2C70F672 FPGA pin-outs alphabetically by signal name and alphabetically by pin number.

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 1 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
1.2V	H10	A10	DIMM_DQ41
1.2V	H11	A11	1.8V
1.2V	H15	A12	GND
1.2V	H16	A13	ADC_A_DCLK
1.2V	H17	A14	USER_RESETN
1.2V	H19	A15	GND
1.2V	H20	A16	1.8V
1.2V	H7	A17	DIMM_DQ61
1.2V	J18	A18	DIMM_DQ56
1.2V	J9	A19	USER_DIPSW1
1.2V	K10	A2	GND
1.2V	K11	A20	ADC_B_D6
1.2V	K12	A21	ADC_A_D9
1.2V	K13	A22	ADC_A_D13
1.2V	K14	A23	ADC_A_D10
1.2V	K15	A24	1.8V
1.2V	K18	A25	GND
1.2V	K9	A3	1.8V
1.2V	L11	A4	DIMM_DM8
1.2V	L16	A5	DIMM_DQ70
1.2V	L17	A6	ADC_B_OVR
1.2V	L18	A7	DIMM_DQ38
1.2V	L9	A8	ADC_A_D3
1.2V	M10	A9	ADC_A_D4
1.2V	M11	AA1	DAC_A_D1

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 2 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
1.2V	M16	AA10	DIMM_DQ25
1.2V	M17	AA11	DIMM_DQ29
1.2V	N10	AA12	DIMM_DM1
1.2V	N17	AA13	DIMM_DQ14
1.2V	P10	AA14	VREF
1.2V	P17	AA15	DIMM_DQ9
1.2V	R10	AA16	DIMM_DQ0
1.2V	R11	AA17	DIMM_WEN_R
1.2V	R16	AA18	DIMM_SCL
1.2V	R19	AA19	VCCA_PLL4
1.2V	R8	AA2	AUDIO_MODE
1.2V	T11	AA20	DIMM_CK_N2
1.2V	T16	AA21	GND
1.2V	T18	AA22	3.3V
1.2V	T19	AA23	EVM_OEN
1.2V	T8	AA24	EVM_D9
1.2V	T9	AA25	EVM_D5
1.2V	U11	AA26	EVM_D7
1.2V	U13	AA3	DIG_LSB_C
1.2V	U14	AA4	VGA_G5
1.2V	U15	AA5	DAC_A_D7
1.2V	U16	AA6	USER_LED6
1.2V	U18	AA7	USER_LED7
1.2V	U9	AA8	VCCA_PLL1
1.2V	V10	AA9	DIMM_DQ31
1.2V	V16	AB1	DAC_A_D0
1.2V	V18	AB10	DIMM_DQ24
1.2V	V9	AB11	GND
1.2V	W10	AB12	DIMM_DQ20
1.2V	W11	AB13	1.8V
1.2V	W15	AB14	1.8V
1.2V	W16	AB15	DIMM_BA_R2



**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 3 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
1.2V	W17	AB16	GND
1.2V	Y20	AB17	1.8V
1.2V	Y7	AB18	DIMM_CSN_R1
1.8V	A11	AB19	GND
1.8V	A16	AB2	AUDIO_LRCOUT
1.8V	A24	AB20	DIMM_CK_P1
1.8V	A3	AB21	DIMM_SYNC_CLK
1.8V	AB13	AB22	1.8V
1.8V	AB14	AB23	DIG_MSB_C
1.8V	AB17	AB24	EVM_D29
1.8V	AB22	AB25	EVM_D1
1.8V	AB6	AB26	EVM_D3
1.8V	AB9	AB3	AUDIO_CLK
1.8V	AD20	AB4	USER_LED5
1.8V	AF11	AB5	3.3V
1.8V	AF16	AB6	1.8V
1.8V	AF24	AB7	GND
1.8V	AF3	AB8	DIMM_A_R7
1.8V	C20	AB9	1.8V
1.8V	D22	AC1	VGA_B0
1.8V	E13	AC10	VREF
1.8V	E14	AC11	DIMM_DQ16
1.8V	E17	AC12	VREF
1.8V	E6	AC13	USER_DIPSW0
1.8V	E9	AC14	DIMM_DQ10
1.8V	H18	AC15	DIMM_DM0
1.8V	H9	AC16	VREF
1.8V	J12	AC17	DIMM_DQ1
1.8V	J15	AC18	USER_PB0
1.8V	V12	AC19	DIMM_CKE_R1
1.8V	V15	AC2	DIG_LSB_G
1.8V	W18	AC20	USER_DIPSW5

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 4 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
1.8V	W9	AC21	DIMM_CK_P0
3.3V	AA22	AC22	DIMM_CASN_R
3.3V	AB5	AC23	VGA_R4
3.3V	AD1	AC24	
3.3V	AD26	AC25	AUDIO_CSN
3.3V	C1	AC26	EVM_INT2
3.3V	C26	AC3	USER_LED4
3.3V	F22	AC4	GND
3.3V	F5	AC5	DIMM_A_R14
3.3V	J19	AC6	DIMM_A_R6
3.3V	L1	AC7	VREF
3.3V	L26	AC8	DIMM_A_R1
3.3V	M18	AC9	DIMM_DM2
3.3V	M9	AD1	3.3V
3.3V	N22	AD10	DIMM_DQ17
3.3V	N5	AD11	DIMM_DQ21
3.3V	P22	AD12	DIMM_DQ11
3.3V	P5	AD13	PROTO_CLKOUT
3.3V	R18	AD14	GND
3.3V	R9	AD15	GND
3.3V	T1	AD16	DIMM_DQ7
3.3V	T26	AD17	DIMM_DQ5
3.3V	V19	AD18	GND
3.3V	V8	AD19	DIMM_CK_N0
ADC_A_D0	C5	AD2	AUDIO_SDIN
ADC_A_D1	C6	AD20	1.8V
ADC_A_D10	A23	AD21	DIMM_CK_N1
ADC_A_D11	B23	AD22	DIMM_CK_P2
ADC_A_D12	C22	AD23	DIMM_RESETN
ADC_A_D13	A22	AD24	ADC_SCLK
ADC_A_D2	B7	AD25	VGA_R2
ADC_A_D3	A8	AD26	3.3V

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 5 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
ADC_A_D4	A9	AD3	DAC_A_D3
ADC_A_D5	C11	AD4	DIMM_A_R11
ADC_A_D6	B12	AD5	DIMM_A_R8
ADC_A_D7	D13	AD6	DIMM_A_R2
ADC_A_D8	B22	AD7	DIMM_A_R5
ADC_A_D9	A21	AD8	DIMM_DM3
ADC_A_DCLK	A13	AD9	GND
ADC_A_OE	F7	AE1	GND
ADC_A_OVR	D15	AE10	DIMM_DQ18
ADC_A_SEN	B18	AE11	DIMM_A_R9
ADC_B_D0	F17	AE12	DIMM_DQ15
ADC_B_D1	D17	AE13	DIMM_DQS2
ADC_B_D10	E18	AE14	USER_PB3
ADC_B_D11	E20	AE15	DIMM_DQS1
ADC_B_D12	D21	AE16	USER_PB1
ADC_B_D13	D20	AE17	DIMM_DQ2
ADC_B_D2	D18	AE18	USER_DIPSW6
ADC_B_D3	C19	AE19	USER_DIPSW7
ADC_B_D4	B19	AE2	VGA_SYNCN
ADC_B_D5	B20	AE20	DIMM_RASN_R
ADC_B_D6	A20	AE21	DIMM_CKE_R0
ADC_B_D7	B21	AE22	USER_PB2
ADC_B_D8	F18	AE23	DIMM_ODT_R1
ADC_B_D9	G18	AE24	
ADC_B_DCLK	C13	AE25	EVM_CEN3
ADC_B_OE	R2	AE26	GND
ADC_B_OVR	A6	AE3	DAC_A_D2
ADC_B_SEN	D19	AE4	DIMM_A_R0
ADC_RESET	T24	AE5	DIMM_A_R10
ADC_SCLK	AD24	AE6	DIMM_DQ26
ADC_SDATA	Y1	AE7	DIMM_DQ27
AUDIO_BCLK	F3	AE8	DIMM_DQS3

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 6 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
AUDIO_CLK	AB3	AE9	DIMM_DQ19
AUDIO_CSN	AC25	AF10	DIMM_DQ22
AUDIO_DIN	J21	AF11	1.8V
AUDIO_DOUT	B13	AF12	GND
AUDIO_LRCIN	W4	AF13	DIMM_A_R15
AUDIO_LRCOUT	AB2	AF14	DIMM_SYNC_CLK
AUDIO_MODE	AA2	AF15	GND
AUDIO_SCLK	R4	AF16	1.8V
AUDIO_SDIN	AD2	AF17	DIMM_DQ3
CLKIN_BOT	N25	AF18	DIMM_DQ6
CLKIN_TOP	N2	AF19	DIMM_DQS0
DAC_A_D0	AB1	AF2	GND
DAC_A_D1	AA1	AF20	DIMM_SDA
DAC_A_D10	P3	AF21	DIMM_ODT_R0
DAC_A_D11	U7	AF22	DIMM_CSN_R0
DAC_A_D12	R5	AF23	DIMM_BA_R1
DAC_A_D13	P6	AF24	1.8V
DAC_A_D2	AE3	AF25	GND
DAC_A_D3	AD3	AF3	1.8V
DAC_A_D4	U3	AF4	USER_DIPSW4
DAC_A_D5	T2	AF5	DIMM_A_R4
DAC_A_D6	Y4	AF6	DIMM_DQ30
DAC_A_D7	AA5	AF7	DIMM_A_R13
DAC_A_D8	V5	AF8	GND
DAC_A_D9	V6	AF9	DIMM_DQ23
DAC_B_D0	M4	B1	GND
DAC_B_D1	M5	B10	DIMM_DQ40
DAC_B_D10	W25	B11	DIMM_DQ52
DAC_B_D11	W26	B12	ADC_A_D6
DAC_B_D12	V25	B13	AUDIO_DOUT
DAC_B_D13	T25	B14	DIMM_DQS6
DAC_B_D2	U20	B15	DIMM_DQ54

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 7 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
DAC_B_D3	V20	B16	DIMM_DQ50
DAC_B_D4	V21	B17	DIMM_DQ57
DAC_B_D5	B24	B18	ADC_A_SEN
DAC_B_D6	T23	B19	ADC_B_D4
DAC_B_D7	P23	B2	VGA_B2
DAC_B_D8	Y24	B20	ADC_B_D5
DAC_B_D9	V24	B21	ADC_B_D7
DIG_LSB_A	K2	B22	ADC_A_D8
DIG_LSB_B	U25	B23	ADC_A_D11
DIG_LSB_C	AA3	B24	DAC_B_D5
DIG_LSB_D	V1	B25	EVM_A20
DIG_LSB_DP	P7	B26	GND
DIG_LSB_E	V7	B3	USER_LED1
DIG_LSB_F	U23	B4	DIMM_DQ69
DIG_LSB_G	AC2	B5	DIMM_DQ66
DIG_MSB_A	Y21	B6	DIMM_DQS8
DIG_MSB_B	T7	B7	ADC_A_D2
DIG_MSB_C	AB23	B8	DIMM_DQS4
DIG_MSB_D	Y5	B9	DIMM_DM5
DIG_MSB_DP	V3	C1	3.3V
DIG_MSB_E	E1	C10	DIMM_DQ45
DIG_MSB_F	U1	C11	ADC_A_D5
DIG_MSB_G	W21	C12	DIMM_DQS5
DIMM_A_R0	AE4	C13	ADC_B_DCLK
DIMM_A_R1	AC8	C14	GND
DIMM_A_R10	AE5	C15	DIMM_DQ55
DIMM_A_R11	AD4	C16	DIMM_DM7
DIMM_A_R12	Y12	C17	DIMM_DQS7
DIMM_A_R13	AF7	C18	GND
DIMM_A_R14	AC5	C19	ADC_B_D3
DIMM_A_R15	AF13	C2	PROTO_IO12
DIMM_A_R2	AD6	C20	1.8V

**Table C–1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 8 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
DIMM_A_R3	Y10	C21	USER_DIPSW2
DIMM_A_R4	AF5	C22	ADC_A_D12
DIMM_A_R5	AD7	C23	USER_DIPSW3
DIMM_A_R6	AC6	C24	EVM_A18
DIMM_A_R7	AB8	C25	EVM_A16
DIMM_A_R8	AD5	C26	3.3V
DIMM_A_R9	AE11	C3	PROTO_IO40
DIMM_BA_R0	Y18	C4	DIMM_DQ65
DIMM_BA_R1	AF23	C5	ADC_A_D0
DIMM_BA_R2	AB15	C6	ADC_A_D1
DIMM_CASN_R	AC22	C7	DIMM_DQ71
DIMM_CK_N0	AD19	C8	DIMM_DQ34
DIMM_CK_N1	AD21	C9	DIMM_DQ39
DIMM_CK_N2	AA20	D1	PROTO_IO14
DIMM_CK_P0	AC21	D10	DIMM_DQ44
DIMM_CK_P1	AB20	D11	VREF
DIMM_CK_P2	AD22	D12	DIMM_DQ46
DIMM_CKE_R0	AE21	D13	ADC_A_D7
DIMM_CKE_R1	AC19	D14	DIMM_DQ49
DIMM_CSN_R0	AF22	D15	ADC_A_OVR
DIMM_CSN_R1	AB18	D16	VREF
DIMM_DM0	AC15	D17	ADC_B_D1
DIMM_DM1	AA12	D18	ADC_B_D2
DIMM_DM2	AC9	D19	ADC_B_SEN
DIMM_DM3	AD8	D2	PROTO_IO29
DIMM_DM4	D6	D20	ADC_B_D13
DIMM_DM5	B9	D21	ADC_B_D12
DIMM_DM6	G12	D22	1.8V
DIMM_DM7	C16	D23	EVM_A14
DIMM_DM8	A4	D24	GND
DIMM_DQ0	AA16	D25	EVM_A12
DIMM_DQ1	AC17	D26	EVM_A10

**Table C–1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 9 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
DIMM_DQ10	AC14	D3	EP2C_CSON
DIMM_DQ11	AD12	D4	GND
DIMM_DQ12	Y13	D5	VREF
DIMM_DQ13	Y14	D6	DIMM_DM4
DIMM_DQ14	AA13	D7	DIMM_DQ67
DIMM_DQ15	AE12	D8	DIMM_DQ33
DIMM_DQ16	AC11	D9	DIMM_DQ35
DIMM_DQ17	AD10	E1	DIG_MSB_E
DIMM_DQ18	AE10	E10	VREF
DIMM_DQ19	AE9	E11	GND
DIMM_DQ2	AE17	E12	DIMM_DQ47
DIMM_DQ20	AB12	E13	1.8V
DIMM_DQ21	AD11	E14	1.8V
DIMM_DQ22	AF10	E15	DIMM_DQ60
DIMM_DQ23	AF9	E16	GND
DIMM_DQ24	AB10	E17	1.8V
DIMM_DQ25	AA10	E18	ADC_B_D10
DIMM_DQ26	AE6	E19	GND
DIMM_DQ27	AE7	E2	PROTO_IO28
DIMM_DQ28	Y11	E20	ADC_B_D11
DIMM_DQ29	AA11	E21	GND_PLL
DIMM_DQ3	AF17	E22	USER_LED3
DIMM_DQ30	AF6	E23	EVM_A8
DIMM_DQ31	AA9	E24	EVM_A6
DIMM_DQ32	F11	E25	EVM_A2
DIMM_DQ33	D8	E26	EVM_A4
DIMM_DQ34	C8	E3	EP2C_ASDO
DIMM_DQ35	D9	E4	GND_PLL
DIMM_DQ36	G10	E5	USER_LED0
DIMM_DQ37	F10	E6	1.8V
DIMM_DQ38	A7	E7	GND
DIMM_DQ39	C9	E8	VREF

**Table C–1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 10 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
DIMM_DQ4	Y16	E9	1.8V
DIMM_DQ40	B10	F1	PROTO_IO15
DIMM_DQ41	A10	F10	DIMM_DQ37
DIMM_DQ42	F12	F11	DIMM_DQ32
DIMM_DQ43	G11	F12	DIMM_DQ42
DIMM_DQ44	D10	F13	VREF
DIMM_DQ45	C10	F14	DIMM_DQ48
DIMM_DQ46	D12	F15	DIMM_DQ62
DIMM_DQ47	E12	F16	DIMM_DQ63
DIMM_DQ48	F14	F17	ADC_B_D0
DIMM_DQ49	D14	F18	ADC_B_D8
DIMM_DQ5	AD17	F19	GND_PLL
DIMM_DQ50	B16	F2	PROTO_IO13
DIMM_DQ51	G14	F20	USER_LED2
DIMM_DQ52	B11	F21	VGA_VSYNC
DIMM_DQ53	G13	F22	3.3V
DIMM_DQ54	B15	F23	EVM_BEN0
DIMM_DQ55	C15	F24	EVM_CLKX0
DIMM_DQ56	A18	F25	EVM_BEN2
DIMM_DQ57	B17	F26	EVM_A21
DIMM_DQ58	G16	F3	AUDIO_BCLK
DIMM_DQ59	G15	F4	PROTO_IO9
DIMM_DQ6	AF18	F5	3.3V
DIMM_DQ60	E15	F6	PROTO_IO3
DIMM_DQ61	A17	F7	ADC_A_OE
DIMM_DQ62	F15	F8	GND_PLL
DIMM_DQ63	F16	F9	DIMM_DQ68
DIMM_DQ64	G9	G1	PROTO_IO16
DIMM_DQ65	C4	G10	DIMM_DQ36
DIMM_DQ66	B5	G11	DIMM_DQ43
DIMM_DQ67	D7	G12	DIMM_DM6
DIMM_DQ68	F9	G13	DIMM_DQ53



**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 11 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
DIMM_DQ69	B4	G14	DIMM_DQ51
DIMM_DQ7	AD16	G15	DIMM_DQ59
DIMM_DQ70	A5	G16	DIMM_DQ58
DIMM_DQ71	C7	G17	GND
DIMM_DQ8	Y15	G18	ADC_B_D9
DIMM_DQ9	AA15	G19	VCCA_PLL2
DIMM_DQS0	AF19	G2	PROTO_IO27
DIMM_DQS1	AE15	G20	GND
DIMM_DQS2	AE13	G21	EVM_DX0
DIMM_DQS3	AE8	G22	EVM_FSX0
DIMM_DQS4	B8	G23	EVM_D28
DIMM_DQS5	C12	G24	EVM_D30
DIMM_DQS6	B14	G25	EVM_CLKR0
DIMM_DQS7	C17	G26	EVM_A17
DIMM_DQS8	B6	G3	PROTO_IO11
DIMM_ODT_R0	AF21	G4	PROTO_IO10
DIMM_ODT_R1	AE23	G5	PROTO_IO8
DIMM_RASN_R	AE20	G6	PROTO_IO2
DIMM_RESETN	AD23	G7	GND
DIMM_SCL	AA18	G8	VCCA_PLL3
DIMM_SDA	AF20	G9	DIMM_DQ64
DIMM_SYNC_CLK	AB21	H1	PROTO_IO18
DIMM_SYNC_CLK	AF14	H10	1.2V
DIMM_WEN_R	AA17	H11	1.2V
EP2C_ASDO	E3	H12	GND
EP2C_CEN	N4	H13	GND
EP2C_CONFIG_DONE	R23	H14	GND
EP2C_CONFIGN	N7	H15	1.2V
EP2C_CSON	D3	H16	1.2V
EP2C_DATA0	N3	H17	1.2V
EP2C_DCLK	N6	H18	1.8V
EP2C_MSEL1	P21	H19	1.2V

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 12 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
EP2C_STATUSN	R22	H2	VGA_B4
EPCS_USER_CSN	Y23	H20	1.2V
EVM_A10	D26	H21	VGA_HSYNC
EVM_A11	J26	H22	GND
EVM_A12	D25	H23	EVM_D24
EVM_A13	K24	H24	EVM_D26
EVM_A14	D23	H25	EVM_A19
EVM_A15	J25	H26	EVM_DR0
EVM_A16	C25	H3	PROTO_IO26
EVM_A17	G26	H4	PROTO_IO34
EVM_A18	C24	H5	GND
EVM_A19	H25	H6	PROTO_IO1
EVM_A2	E25	H7	1.2V
EVM_A20	B25	H8	GND
EVM_A21	F26	H9	1.8V
EVM_A3	L24	J1	PROTO_IO19
EVM_A4	E26	J10	GND
EVM_A5	L25	J11	GND
EVM_A6	E24	J12	1.8V
EVM_A7	K26	J13	GND
EVM_A8	E23	J14	GND
EVM_A9	K25	J15	1.8V
EVM_ARDY	W23	J16	GND
EVM_AREN	P26	J17	GND
EVM_BEN0	F23	J18	1.2V
EVM_BEN1	M23	J19	3.3V
EVM_BEN2	F25	J2	PROTO_IO20
EVM_BEN3	M24	J20	EVM_FSR0
EVM_BWEN	V23	J21	AUDIO_DIN
EVM_CEN2	J24	J22	EVM_D20
EVM_CEN3	AE25	J23	EVM_D22
EVM_CLKOUT2	P2	J24	EVM_CEN2

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 13 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
EVM_CLKR0	G25	J25	EVM_A15
EVM_CLKX0	F24	J26	EVM_A11
EVM_CNTL0	M21	J3	PROTO_IO17
EVM_D0	V22	J4	PROTO_IO33
EVM_D1	AB25	J5	PROTO_IO0
EVM_D10	L21	J6	PROTO_IO37
EVM_D11	Y26	J7	PROTO_IO31
EVM_D12	K19	J8	PROTO_IO7
EVM_D13	W24	J9	1.2V
EVM_D14	K21	K1	PROTO_IO21
EVM_D15	U22	K10	1.2V
EVM_D16	K22	K11	1.2V
EVM_D17	V26	K12	1.2V
EVM_D18	K23	K13	1.2V
EVM_D19	U24	K14	1.2V
EVM_D2	M19	K15	1.2V
EVM_D20	J22	K16	GND
EVM_D21	U26	K17	GND
EVM_D22	J23	K18	1.2V
EVM_D23	T21	K19	EVM_D12
EVM_D24	H23	K2	DIG_LSB_A
EVM_D25	R24	K20	GND
EVM_D26	H24	K21	EVM_D14
EVM_D27	P24	K22	EVM_D16
EVM_D28	G23	K23	EVM_D18
EVM_D29	AB24	K24	EVM_A13
EVM_D3	AB26	K25	EVM_A9
EVM_D30	G24	K26	EVM_A7
EVM_D31	N23	K3	PROTO_IO25
EVM_D4	N20	K4	PROTO_IO35
EVM_D5	AA25	K5	PROTO_IO32
EVM_D6	M20	K6	PROTO_IO38

**Table C-1. Cyclone II EP2C70F672-G6ES FPGA Pin-Outs (Part 14 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
EVM_D7	AA26	K7	PROTO_IO6
EVM_D8	L19	K8	PROTO_IO39
EVM_D9	AA24	K9	1.2V
EVM_DMAC0	N24	L1	3.3V
EVM_DR0	H26	L10	GND
EVM_DX0	G21	L11	1.2V
EVM_FSR0	J20	L12	GND
EVM_FSX0	G22	L13	GND
EVM_IACK	N26	L14	GND
EVM_INT0	M22	L15	GND
EVM_INT1	M25	L16	1.2V
EVM_INT2	AC26	L17	1.2V
EVM_INT3	L23	L18	1.2V
EVM_INUM0	P1	L19	EVM_D8
EVM_OEN	AA23	L2	PROTO_IO22
EVM_RESET	P25	L20	EVM_STAT0
EVM_STAT0	L20	L21	EVM_D10
FPGA_TO_ADC_CLK	T3	L22	GND
FPGA_TO_DAC_CLK	Y3	L23	EVM_INT3
GND	A12	L24	EVM_A3
GND	A15	L25	EVM_A5
GND	A2	L26	3.3V
GND	A25	L3	PROTO_IO30
GND	AB11	L4	PROTO_IO36
GND	AB16	L5	GND
GND	AB19	L6	PROTO_IO4
GND	AB7	L7	PROTO_IO5
GND	AC4	L8	JTAG_TMS
GND	AD14	L9	1.2V
GND	AD15	M1	GND
GND	AD18	M10	1.2V
GND	AD9	M11	1.2V

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 15 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
GND	AE1	M12	GND
GND	AE26	M13	GND
GND	AF12	M14	GND
GND	AF15	M15	GND
GND	AF2	M16	1 . 2V
GND	AF25	M17	1 . 2V
GND	AF8	M18	3 . 3V
GND	B1	M19	EVM_D2
GND	B26	M2	PROTO_IO24
GND	C14	M20	EVM_D6
GND	C18	M21	EVM_CNTL0
GND	D24	M22	EVM_INT0
GND	D4	M23	EVM_BEN1
GND	E11	M24	EVM_BEN3
GND	E16	M25	EVM_INT1
GND	E19	M26	GND
GND	E7	M3	PROTO_IO23
GND	G17	M4	DAC_B_D0
GND	G20	M5	DAC_B_D1
GND	G7	M6	JTAG_TCK
GND	H12	M7	JTAG_CONN_TDI
GND	H13	M8	JTAG_CONN_TDO
GND	H14	M9	3 . 3V
GND	H22	N1	GND
GND	H5	N10	1 . 2V
GND	H8	N11	GND
GND	J10	N12	GND
GND	J11	N13	GND
GND	J13	N14	GND
GND	J14	N15	GND
GND	J16	N16	GND
GND	J17	N17	1 . 2V

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 16 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
GND	K16	N18	GND
GND	K17	N19	GND
GND	K20	N2	CLKIN_TOP
GND	L10	N20	EVM_D4
GND	L12	N21	
GND	L13	N22	3.3V
GND	L14	N23	EVM_D31
GND	L15	N24	EVM_DMACH0
GND	L22	N25	CLKIN_BOT
GND	L5	N26	EVM_IACK
GND	M1	N3	EP2C_DATA0
GND	M12	N4	EP2C_CEN
GND	M13	N5	3.3V
GND	M14	N6	EP2C_DCLK
GND	M15	N7	EP2C_CONFIGN
GND	M26	N8	GND
GND	N1	N9	GND
GND	N11	P1	EVM_INUM0
GND	N12	P10	1.2V
GND	N13	P11	GND
GND	N14	P12	GND
GND	N15	P13	GND
GND	N16	P14	GND
GND	N18	P15	GND
GND	N19	P16	GND
GND	N8	P17	1.2V
GND	N9	P18	GND
GND	P11	P19	GND
GND	P12	P2	EVM_CLKOUT2
GND	P13	P20	GND
GND	P14	P21	EP2C_MSEL1
GND	P15	P22	3.3V

**Table C-1. Cyclone II EP2C70F672-G6ES FPGA Pin-Outs (Part 17 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
GND	P16	P23	DAC_B_D7
GND	P18	P24	EVM_D27
GND	P19	P25	EVM_RESET
GND	P20	P26	EVM_AREN
GND	P8	P3	DAC_A_D10
GND	P9	P4	VGA_R6
GND	R1	P5	3.3V
GND	R12	P6	DAC_A_D13
GND	R13	P7	DIG_LSB_DP
GND	R14	P8	GND
GND	R15	P9	GND
GND	R17	R1	GND
GND	R21	R10	1.2V
GND	R26	R11	1.2V
GND	T10	R12	GND
GND	T12	R13	GND
GND	T13	R14	GND
GND	T14	R15	GND
GND	T15	R16	1.2V
GND	T17	R17	GND
GND	T5	R18	3.3V
GND	U10	R19	1.2V
GND	U12	R2	ADC_B_OE
GND	U17	R20	PROTO_CLKIN
GND	U19	R21	GND
GND	U8	R22	EP2C_STATUSN
GND	V11	R23	EP2C_CONFIG_DONE
GND	V13	R24	EVM_D25
GND	V14	R25	SRAM_CLK
GND	V17	R26	GND
GND	W12	R3	VGA_G0
GND	W13	R4	AUDIO_SCLK

**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 18 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
GND	W14	R5	DAC_A_D12
GND	W19	R6	VGA_G4
GND	W20	R7	VGA_G2
GND	W22	R8	1.2V
GND	W5	R9	3.3V
GND	W7	T1	3.3V
GND	W8	T10	GND
GND	Y17	T11	1.2V
GND	Y9	T12	GND
GND_PLL	AA21	T13	GND
GND_PLL	E21	T14	GND
GND_PLL	E4	T15	GND
GND_PLL	F19	T16	1.2V
GND_PLL	F8	T17	GND
GND_PLL	Y19	T18	1.2V
GND_PLL	Y6	T19	1.2V
GND	Y8	T2	DAC_A_D5
JTAG_CONN_TDI	M7	T20	VGA_R3
JTAG_CONN_TDO	M8	T21	EVM_D23
JTAG_TCK	M6	T22	VGA_R1
JTAG_TMS	L8	T23	DAC_B_D6
PROTO_CARDSELN	V2	T24	ADC_RESET
PROTO_CLKIN	R20	T25	DAC_B_D13
PROTO_CLKOUT	AD13	T26	3.3V
PROTO_IO0	J5	T3	FPGA_TO_ADC_CLK
PROTO_IO1	H6	T4	VGA_CLK
PROTO_IO10	G4	T5	GND
PROTO_IO11	G3	T6	VGA_G6
PROTO_IO12	C2	T7	DIG_MSB_B
PROTO_IO13	F2	T8	1.2V
PROTO_IO14	D1	T9	1.2V
PROTO_IO15	F1	U1	DIG_MSB_F



**Table C-1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 19 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
PROTO_IO16	G1	U10	GND
PROTO_IO17	J3	U11	1.2V
PROTO_IO18	H1	U12	GND
PROTO_IO19	J1	U13	1.2V
PROTO_IO2	G6	U14	1.2V
PROTO_IO20	J2	U15	1.2V
PROTO_IO21	K1	U16	1.2V
PROTO_IO22	L2	U17	GND
PROTO_IO23	M3	U18	1.2V
PROTO_IO24	M2	U19	GND
PROTO_IO25	K3	U2	VGA_B7
PROTO_IO26	H3	U20	DAC_B_D2
PROTO_IO27	G2	U21	VGA_R5
PROTO_IO28	E2	U22	EVM_D15
PROTO_IO29	D2	U23	DIG_LSB_F
PROTO_IO3	F6	U24	EVM_D19
PROTO_IO30	L3	U25	DIG_LSB_B
PROTO_IO31	J7	U26	EVM_D21
PROTO_IO32	K5	U3	DAC_A_D4
PROTO_IO33	J4	U4	VGA_B6
PROTO_IO34	H4	U5	VGA_G3
PROTO_IO35	K4	U6	VGA_BLANKN
PROTO_IO36	L4	U7	DAC_A_D11
PROTO_IO37	J6	U8	GND
PROTO_IO38	K6	U9	1.2V
PROTO_IO39	K8	V1	DIG_LSB_D
PROTO_IO4	L6	V10	1.2V
PROTO_IO40	C3	V11	GND
PROTO_IO5	L7	V12	1.8V
PROTO_IO6	K7	V13	GND
PROTO_IO7	J8	V14	GND
PROTO_IO8	G5	V15	1.8V

**Table C–1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 20 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
PROTO_IO9	F4	V16	1.2V
SRAM_CLK	R25	V17	GND
USER_DIPSW0	AC13	V18	1.2V
USER_DIPSW1	A19	V19	3.3V
USER_DIPSW2	C21	V2	PROTO_CARDSELN
USER_DIPSW3	C23	V20	DAC_B_D3
USER_DIPSW4	AF4	V21	DAC_B_D4
USER_DIPSW5	AC20	V22	EVM_D0
USER_DIPSW6	AE18	V23	EVM_BWEN
USER_DIPSW7	AE19	V24	DAC_B_D9
USER_LED0	E5	V25	DAC_B_D12
USER_LED1	B3	V26	EVM_D17
USER_LED2	F20	V3	DIG_MSB_DP
USER_LED3	E22	V4	VGA_G7
USER_LED4	AC3	V5	DAC_A_D8
USER_LED5	AB4	V6	DAC_A_D9
USER_LED6	AA6	V7	DIG_LSB_E
USER_LED7	AA7	V8	3.3V
USER_PB0	AC18	V9	1.2V
USER_PB1	AE16	W1	VGA_B5
USER_PB2	AE22	W10	1.2V
USER_PB3	AE14	W11	1.2V
USER_RESETN	A14	W12	GND
VCCA_PLL1	AA8	W13	GND
VCCA_PLL2	G19	W14	GND
VCCA_PLL3	G8	W15	1.2V
VCCA_PLL4	AA19	W16	1.2V
VGA_B0	AC1	W17	1.2V
VGA_B1	W3	W18	1.8V
VGA_B2	B2	W19	GND
VGA_B3	W2	W2	VGA_B3
VGA_B4	H2	W20	GND

**Table C–1. Cyclone II EP2C70F672-C6ES FPGA Pin-Outs (Part 21 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
VGA_B5	W1	W21	DIG_MSB_G
VGA_B6	U4	W22	GND
VGA_B7	U2	W23	EVM_ARDY
VGA_BLANKN	U6	W24	EVM_D13
VGA_CLK	T4	W25	DAC_B_D10
VGA_G0	R3	W26	DAC_B_D11
VGA_G1	W6	W3	VGA_B1
VGA_G2	R7	W4	AUDIO_LRCIN
VGA_G3	U5	W5	GND
VGA_G4	R6	W6	VGA_G1
VGA_G5	AA4	W7	GND
VGA_G6	T6	W8	GND
VGA_G7	V4	W9	1.8V
VGA_HSYNC	H21	Y1	ADC_SDATA
VGA_R0	Y22	Y10	DIMM_A_R3
VGA_R1	T22	Y11	DIMM_DQ28
VGA_R2	AD25	Y12	DIMM_A_R12
VGA_R3	T20	Y13	DIMM_DQ12
VGA_R4	AC23	Y14	DIMM_DQ13
VGA_R5	U21	Y15	DIMM_DQ8
VGA_R6	P4	Y16	DIMM_DQ4
VGA_R7	Y25	Y17	GND
VGA_SYNCN	AE2	Y18	DIMM_BA_R0
VGA_VSYNC	F21	Y19	GND_PLL
VREF	AA14	Y2	
VREF	AC10	Y20	1.2V
VREF	AC12	Y21	DIG_MSB_A
VREF	AC16	Y22	VGA_R0
VREF	AC7	Y23	EPCS_USER_CSN
VREF	D11	Y24	DAC_B_D8
VREF	D16	Y25	VGA_R7
VREF	D5	Y26	EVM_D11

**Table C-1. Cyclone II EP2C70F672-G6ES FPGA Pin-Outs (Part 22 of 22) Note (1)**

Alphabetical by Signal Name		Alphabetical by Pin Number	
Schematic Signal Name	Pin Number	Pin Number	Schematic Signal Name
VREF	E10	Y3	FPGA_TO_DAC_CLK
VREF	E8	Y4	DAC_A_D6
VREF	F13	Y5	DIG_MSB_D
	AC24	Y6	GND_PLL
	AE24	Y7	1.2V
	N21	Y8	GND_PLL

**Note to Table C-1:**

(1) Blank cells indicate no connection.

## Introduction

This appendix provides the following information:

- “Factory-Programmed Factory Design”
- “User Designs”
- “Reprogramming the Factory Design to the EPSC64 Device (U17)”

### Factory-Programmed Factory Design

The Cyclone™ II DSP development board is factory programmed with a factory design stored in flash memory, the EPCS64 (SAFE EPCS) serial configuration device (U17). When power is applied to the board, the on-board logic downloads the factory design to configure the EP2C70 FPGA.

### User Designs

The EPCS64 serial configuration device (U36) is used to store a user design. When power is applied to the board, the on-board logic downloads the user design to configure the EP2C70 FPGA.

### Reprogramming the Factory Design to the EPSC64 Device (U17)

During the development process, you may accidentally overwrite the factory design in the EPCS64 (SAFE EPCS) flash memory serial configuration device (U17). Altera includes the Programmer Object File (.pof) factory design in the *DSP Development Kit, Cyclone II Edition*, so you can reprogram the Cyclone II DSP development board to the original factory configuration.

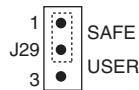
To reprogram the EPCS64 (U17), follow these steps:

1. Set SAFE EPCS mode by placing a jumper on pins 1 and 2 on J29. See [Figure D-1](#) and

**Figure D-1. Setting SAFE EPCS Mode on J29**



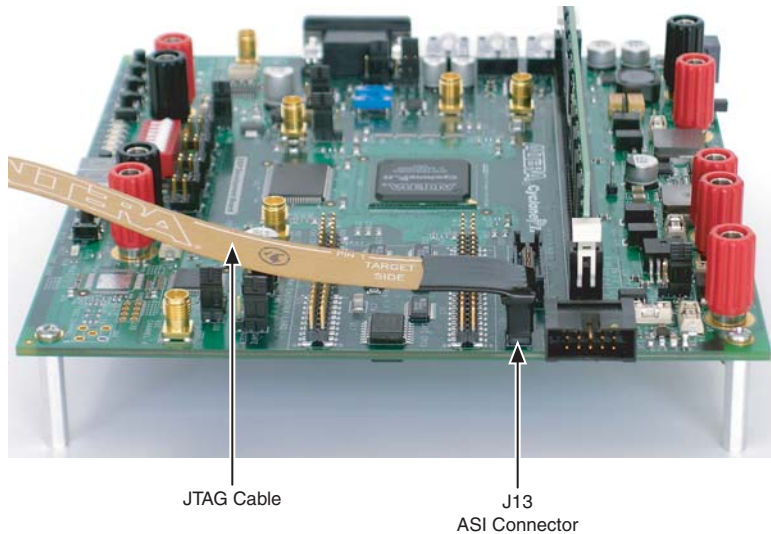
**Figure D-2. J29 SAFE Mode Setting**



2. Connect the USB-Blaster™ download cable to the active serial interface (ASI) connector (J13). Connect the other end of the cable to the USB port on your PC, as shown in [Figure D-3](#).

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**Figure D-3. The JTAG Cable Connected to the ASI Connector J13**



3. Run the Quartus II software
4. Select **Programmer** (Tools menu).
5. In the **Mode** box, select **Active Serial Programming**, click **Add File**.
6. Browse to the directory:

`<install-path>\CycloneII_DSP_Kit-v6.0.1\Examples\  
FactoryDesign_ChA.`



Software and hardware installation and setup are described in the *DSP Development Kit, Cyclone II Edition Getting Started User Guide*.

7. Select **sines.pof** and click **Open**.
8. Turn on **Program/Configure** and click **Start** to program the EPCS64. When the **Progress** bar reaches 100%, programming is complete.
9. Press SYS RESET (SW7) to reset the hardware and reconfigure the Cyclone II DSP development board in SYS RESET mode. You should see the POWER LED (D1) turn on, indicating power is present, the LEDs D2 through D5 (USER\_LED0 through USER\_LED4,

respectively), flash yellow, functioning as a binary counter that counts down to zero. This indicates that the Cyclone II DSP development board is functional and the EP2C70 FPGA was successfully configured with the factory design.