Precision Analog Microcontroller
ARM Cortex M3, with 12-bit ADC & RF

Anomaly List

ADuCRF101

The ADuCRF101 documentation set, datasheet and user manual, describe the final ADuCRF101 device.

Second samples of ADuCRF101 are slightly different to the final product and this document describes the differences between second and final silicon. It also includes the known bugs, anomalies, and workarounds for the ADuCRF101 precision analog microcontroller.

The differences listed apply to all ADuCRF101 packaged material branded as follows:

First Line ADUCRF101
Second Line BSPZ128
Third Line B3W

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADUCRF101 SILICON DIFFERENCES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		B3W	Pre Release	PrB	5

ADUCRF101 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		B3W	Pre Release	PrB	2

ADUCRF101 PERFORMANCE ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		B3W	Pre Release	PrB	1

Rev. Pr B

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SECTION 1: SILICON DIFFERENCES

1. [dif01]: Low power mode 6

Background:	The ADuCRF101 has 6 low power modes, the lowest being the non-retained state with a current consumption of ~500nA.
Issue :	On second silicon the non-retained state is not available. The lowest mode is TOTAL-HALT mode, with ~1uA current consumption.
Workaround:	Use TOTAL-HALT mode.
Related Issues:	None.

2. [dif02]: 16MHz trim block

Background:	The ADuCRF101 operates from an on-chip oscillator generating an internal 16MHz high frequency clock, with ±3% accuracy typically. The frequency of the oscillator can be trimmed by user code.
Issue :	On second silicon the trim feature is not available.
Workaround:	None.
Related Issues:	None.

3. [dif03]: RF test modes

Background:	To check performance on users PCB, some RF test modes are available to the user.
Issue :	On second silicon these modes are not available.
Workaround:	None.
Related Issues:	None.

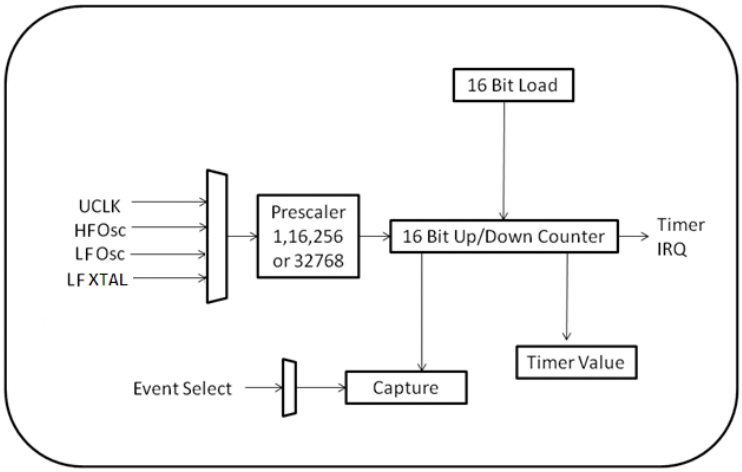
4. [dif04]: Serial wire debug

Background:	The Serial Wire interface is available on SWDIO and SWCK. P1.2 and P1.3 in mode 0 also reflect serial wire signals.
Issue :	On second silicon, by default, P1.2 and P1.3 are configured in mode 0, and Serial Wire activity is reflected on these two pins when debugging/downloading using the dedicated SWD pins. P1.2 and P1.3 have no effect on debug/download when configured in mode 0.
Workaround :	User code should configure P1.2 and P1.3 to GPIO mode, mode 1.
Related Issues:	

5. [dif05]: General Purpose Timer Clock Source

Background: General Purpose Timer 0 And General Purpose Timer 1 have 4 selectable clock sources.

Issue : On second silicon the General Purpose Timer clock sources are slightly different.
Second Silicon: General Purpose Timer Block Diagram:



Register bits	Value	Clock Source
T0CON[6:5] and T1CON[6:5], Clock Select	00	UCLK
T0CON[6:5] and T1CON[6:5], Clock Select	01	HFOSC
T0CON[6:5] and T1CON[6:5], Clock Select	10	LFOSC
T0CON[6:5] and T1CON[6:5], Clock Select	11	LFXTAL

Workaround :

Related Issues:

SECTION 2: FUNCTIONALITY ISSUES

1. RC Oscillator Accuracy [er001]

Background	The RC oscillator can be used to control the wake-up timing of the ADF7023 low power modes. Its typical accuracy is specified as 1.5% after a calibration at 25°C.
Issue	The calibration range of the RC oscillator is not sufficient to ensure a 1.5% typical accuracy on all devices. This can result in the post calibration accuracy on some devices being significantly greater than 1.5%.
Workaround	For applications requiring accurate low power mode timing, the 32.768 kHz external oscillator should be used.
Related Issues	None

2. Optimum Uncalibrated Image Attenuation [er002]

Background	The typical uncalibrated image attenuation is specified as 40 dB at 433 MHz and 36 dB at 868 MHz/915MHz.
Issue	To achieve the typical uncalibrated image attenuation values specified in the datasheet, it is required to use recommended default values for IMAGE_REJECT_CAL_PHASE (Address 0x118) and IMAGE_REJECT_CAL_AMPLITUDE (Address 0x119).
Workaround	To achieve the specified uncalibrated image attenuation at 433 MHz, set IMAGE_REJECT_CAL_AMPLITUDE = 0 and IMAGE_REJECT_CAL_PHASE = 14. To achieve the specified uncalibrated image attenuation at 868 MHz/915 MHz, set IMAGE_REJECT_CAL_AMPLITUDE = 8 and IMAGE_REJECT_CAL_PHASE = 55.
Related Issues	None

SECTION 3: PERFORMANCE ISSUES

Receiver Sensitivity At 910MHz [er003]

Background	The 910 MHz channel falls exactly on the 35th harmonic of the 26 MHz crystal reference.
Issue	When the UHF Transceiver is configured for reception at 910 MHz ± (IF bandwidth × 2), the receiver sensitivity can be degraded by up to 20 dB.
Workaround	The degradation in receiver sensitivity at 910 MHz± (IF bandwidth × 2) can be significantly improved by using the following configuration: 1. Disable the AGC by setting AGC_LOCK_MODE (in Register RADIO_CFG_7, Address 0x113) = 0x01. 2. Set the receiver gain to maximum by setting AGC_MODE (Address 0x35D) = 0x36. 3. Disable the ADC by writing 0x0F to MCR Register 0x324.
Related Issues	None.

SECTION 1. ADUCRF101 SILICON DIFFERENCES

Reference Number	Description	Status
Dif01	Low power mode 6	Open
Dif02	16MHz trim block	Open
Dif03	RF test modes	Open
Dif04	Serial Wire debug	Open
Dif05	General Purpose Timer Clock Source	Open

SECTION 2. ADUCRF101 FUNCTIONALITY ISSUES

Reference Number	Description	Status
Er001	RC Oscillator Accuracy	Open
Er002	Optimum uncalibrated Image Attenuation	Open

SECTION 3. ADUCRF101 PERFORMANCE ISSUES

Reference Number	Description	Status
Er003	Receiver Sensitivity at 910MHz	Open