Instructions for Tele-Training

Prior to the start of the class:

- Download the latest PSoC Designer software at http://www.cypress.com/support/link.cfm?sd=4.
- If you have a PSoC ICE, connect it to your computer.
- Visit http://cypress.webex.com, select a training session under the “Today” or “Upcoming” tab, and follow the instructions to register. After you register you’ll receive an email with directions on how to join your session. ***(NOTE: IT IS BEST TO REGISTER AT LEAST ONE DAY IN ADVANCE.)***

If you have questions or need assistance, please call us toll free at 800.669.0557 (425.787.4400 for local calls or calls outside North America).

CYPRESS

Connecting From Last Mile to First Mile.™

Module 1: Introduction to PSoC

PERSONAL ACCESS ENTERPRISE METRO CORE

Module Objectives

Section 1: Introduction to Cypress Semiconductor & PSoC

Section 2: PSoC Designer™ IDE Software

- PSoC In-Circuit Emulator (ICE)

Section 3: Hands-On System Design with PSoC

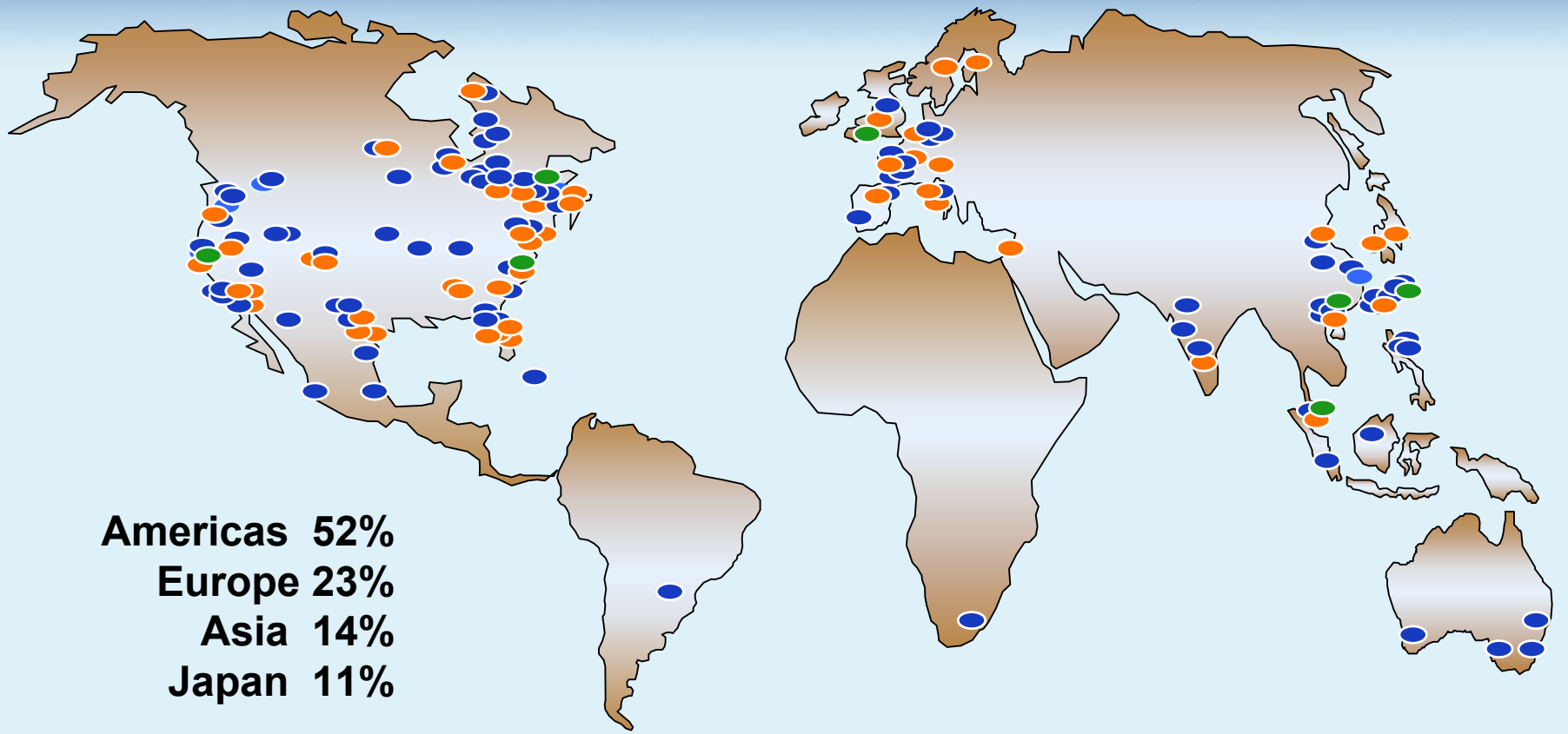
- Defining System Requirements
- Choosing User Modules
- Placing User Modules
- Setting Global and User Module Parameters
- Defining the Pin-out of Your Design
- Generating Your Application
- Reviewing Generated Application Code
- Simple Debugging

Section 4: Cypress MicroSystems Commitment to Support

Cypress Fundamentals

- A diversified semiconductor supplier with a strong systems & communications focus.
- 4,000 employees worldwide
- Headquarters in San Jose, California (NYSE: CY)
- 2002 Revenue: $775M
- Founded in 1982 by CEO T.J. Rodgers
- Cypress is known in the semiconductor industry for its cutting-edge innovation, as well as superior product design, manufacturing, and quality.

Cypress Global Sales

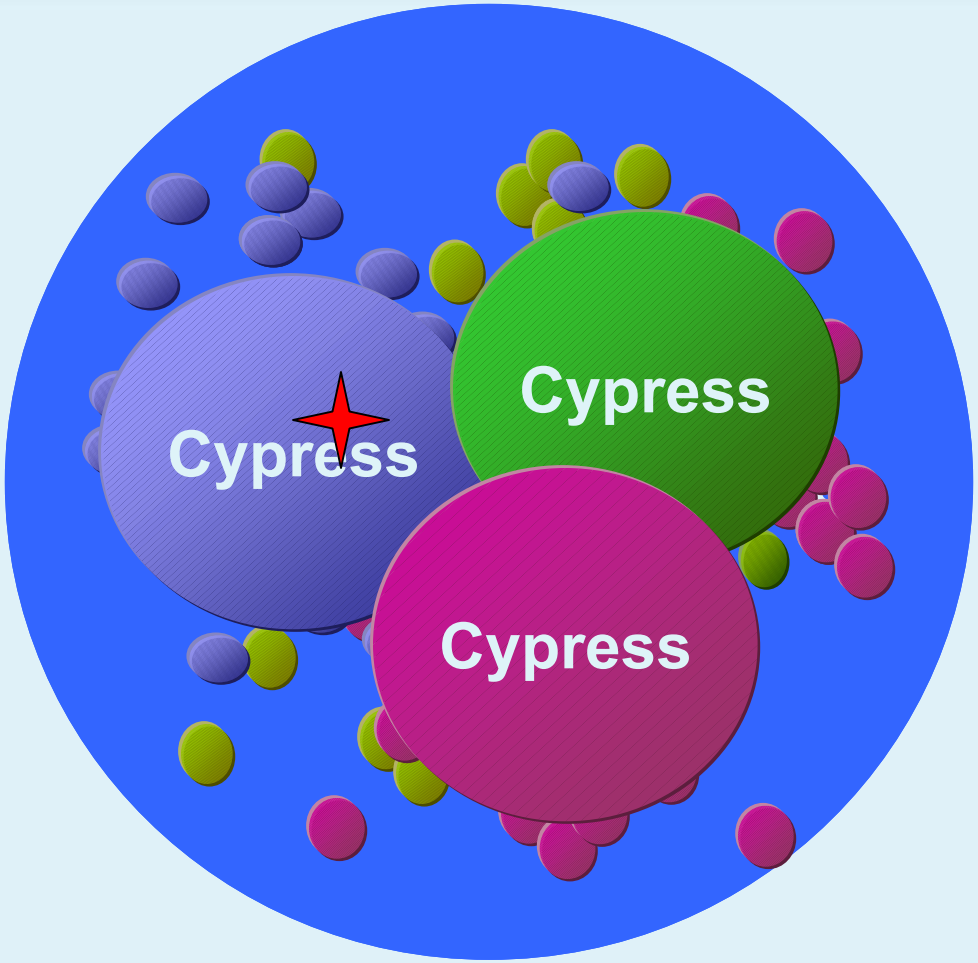


Americas 52%
Europe 23%
Asia 14%
Japan 11%

- Direct Sales Office (58)
- Representative Sales Offices (44)
- Customer Design Centers (7)

> 500+ Person Team

Microcontroller Market



Current Embedded Marketplace:

- Each part covers small functionality
- Families tend to cluster; second sourcing leads to overlaps
- Customers believe they need custom micros

Cypress Strategy:

- Provide part numbers that *each* cover **MORE functionality** (i.e., cover hundreds of competitive devices)

Decrease System Costs

Traditional CO Solution

8-bit Micro	$2.00
Crystal + Caps	$0.57
Filters	$0.30
Amps	$0.20
Speaker Driver	$0.15
LED Drivers	$0.05
Circuit Board	$1.20
Assembly	$1.60

System BOM = **$6.07**

Cypress CO Solution

PSoC Micro.	$2.50
Circuit Board	$0.90
Assembly	$1.40

PSoC BOM = **$4.80**

Connecting From Last Mile to First Mile™

PSoC = Programmable System-on-Chip

- PSoC is a configurable mixed signal array with an on board controller.
- Create your customized chip.

User Defines:

What Functions Appear

When They Appear

How They Interconnect

Example of "What Functions Appear"

PSoC can be defined to meet customer requirements with Countless configuration possibilities

Both of these devices are made from the **same chip!**

Device 1

- One 8-Bit Counter
- One 16-Bit Timer
- One Full-Duplex UART w/Baud Rate Generator
- One SPI Slave (Full Duplex)
- One 4-Input 8-Bit Delta-Sigma A/D
- One 6-Bit D/A
- One 8-Bit D/A
- Two Low-Pass Filters

Device 2

- One 16-Bit Counter
- One 8-Bit PWM
- One Half-Duplex UART
- One SPI Master
- One 12-Bit Incremental A/D
- One Low-Pass Filter
- One 8-Bit D/A
- Two Instrumentation Amplifiers

"When Functions Appear"
In-Application Reuse of Resources

Dynamic Reconfiguration allows multiple function sets to operate on the ***SAME CHIP*** at ***DIFFERENT TIMES*** in the ***SAME APPLICATION***

Example:

23 Hours 59 minutes per day

- Accepts Money
- Distributes Beverages

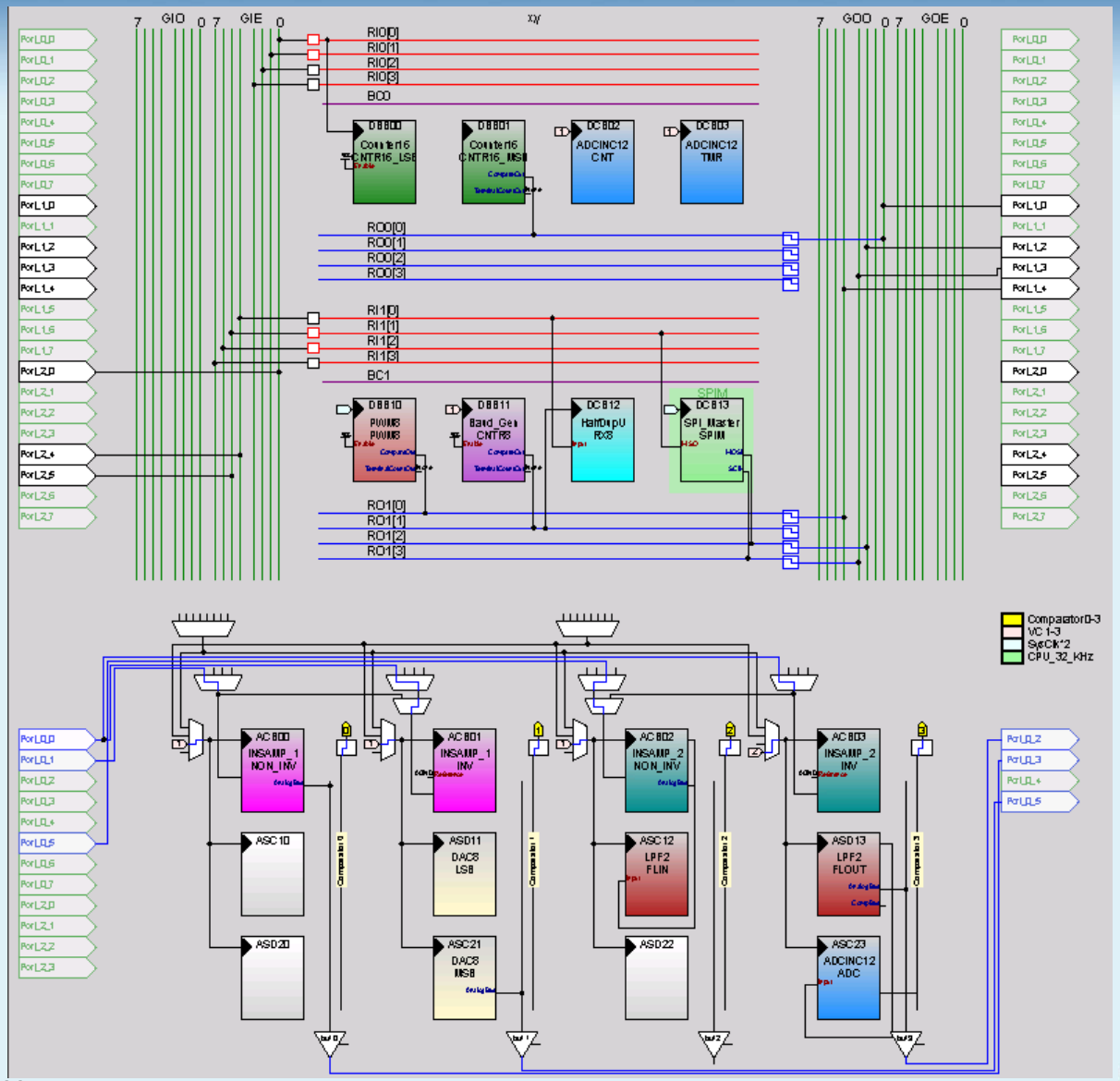
A few seconds each night

- Dynamically reconfigures into a 300 baud Modem
- Transmits coin, beverage and maintenance status to central office

Benefits

- Only cost delta is phone interface
- Increased machine profitability

How They Interconnect



- Define connections between pins and function blocks
- Define connections between function blocks
- Define clock paths
- Change connections dynamically too!

World-Class Features

Cypress Enhanced Analog (CEA)

- Rail-to-rail inputs
- Low opamp input offset (5 mV)
- Low opamp noise (80 nV/rtHz) and low ground path noise
- 8 selectable analog reference points
- Low power comparator (< 15 uA)
- Differential inputs on opamps
- PGA gain up to 48x
- Three opamp instrumentation amp topology

World-Class Features

- Embedded M8C Microprocessor Core
  - Programmable processor speeds
    - Up to 24 MHz (4 MIPs) Operation at 5V
    - Up to 12 MHz Operation at 3.3V
  - Harvard architecture
  - Used in Cypress USB products
- Single-cell (1.2V to start) Operation at up to 24MHz
  - with Built-in Voltage Pump and three passive components
- Internal system supervisor for PSoC
  - Eight-level Low Voltage Detection/Alert
- 2.5% Accurate Oscillator with no ext. components
  - PLL for precise time-base with inexpensive watch crystal
- Flexible Sleep Modes, as low as 3.0µA in Standby

World-Class Features

- 16 KBytes Flash Program Memory
- EEPROM Emulation in Flash
- 256 Bytes SRAM
  - User defined stack length
- Built-In Multiply-Accumulate Hardware (MAC)
  - 8 X 8 Multiply, 32-bit Accumulate
  - Answer available immediately on next instruction cycle
- Four Memory Protection Modes
  - Allows factory or field upgrade on individual 64-byte blocks
  - From one block up to the entire Flash memory protectable
  - Robust read/write protection algorithm for added security
- In-System Serial Programmable (ISSP™)
  - Supports BIST or production test/calibration re-programming
  - Recommended that ISSP interface be designed into PCB

World-Class Features

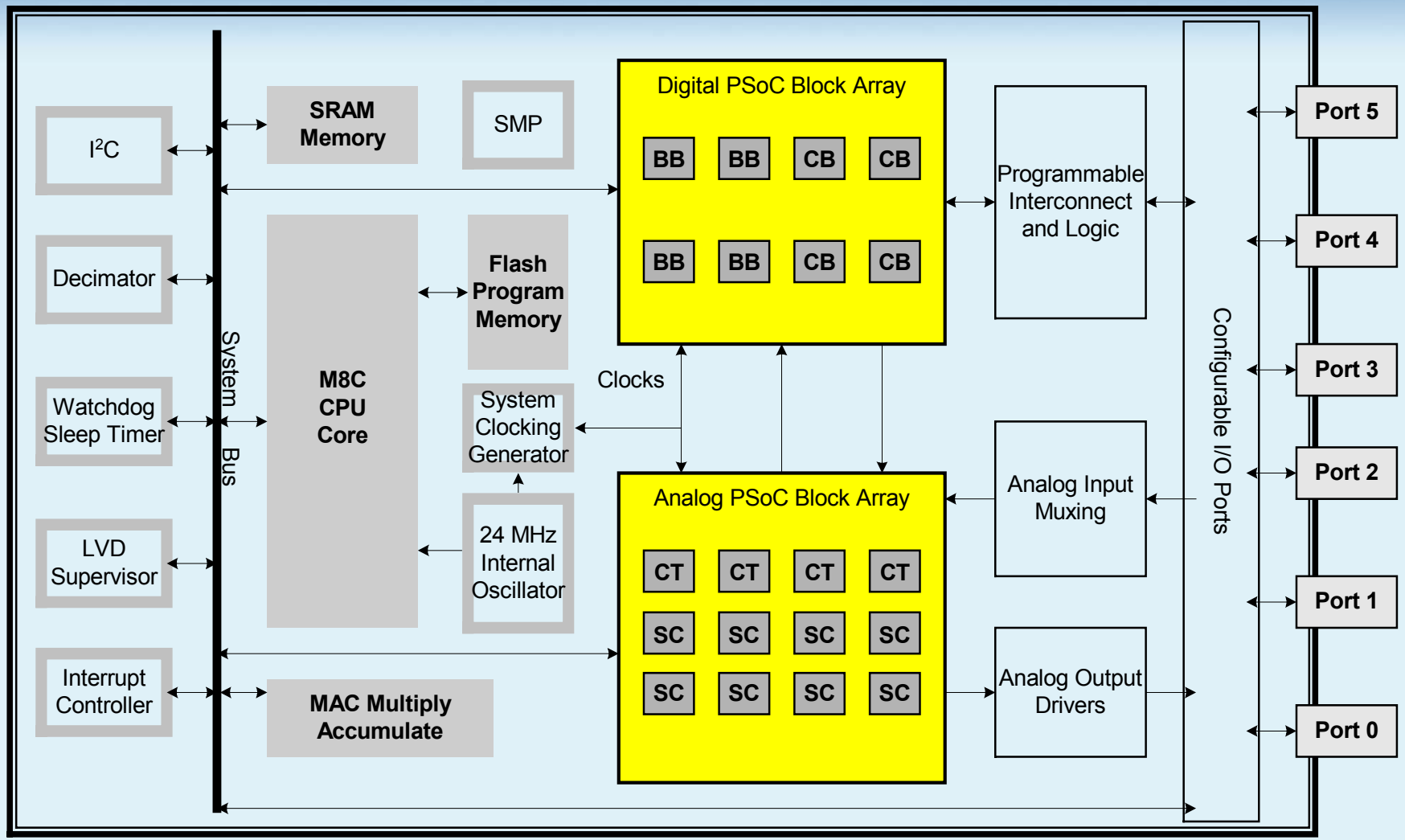
- Configurable I/O Pins
  - Every pin can source 10mA and sink 25mA
  - Integrated/selectable pull-up and pull-down resistors
  - Selectable as interrupt source on either edge/change in state
  - Analog input with Schmitt trigger disabled
    - Disconnect logical inputs for lower digital feedback noise
    - Reduced noise level at nominal logic threshold
  - Slope controlled strong output
    - Reduced current transients, slower rise times for reduced radiated emissions
  - Open Drain and Open Source outputs (actually open-drain N-channel and open-drain P-channel)
- 8 Muxable Analog Inputs (except 8-pin device)
- 4 Analog Outputs each w/ 40mA drive
- 4 direct input analog lines (except 8-pin device)

Sleep Power Comparison

With sleep resources enabled, PSoC is #1

	PSoC	Comp a	Comp b	Comp c	Comp d
Basic sleep current	3uA	1uA	0.1uA	0.5uA	2uA
Rank	5	2	1	3	4
Conditions	POR, WDT, -40-85'C, 3.3V	25'C, 1.8V	Osc, 25'C, 3.0V	All off, -40-85'C, 2.5V	All off, 25'C, 3.3V
POR	Included	+20uA at 3.3V	+10uA at 3.0V	+45uA at 2.5V	+188uA at 3.3V
Sleep/Osc	Included	+7uA at 3.3V	+1.5uA at 3.0V	+15uA at 2.5V	+10uA at 3.3V
WDT	Included	+7uA at 3.3V	Not provided	+1uA at 2.5V	Not provided
Total	3uA	35uA	12uA	61uA	200uA
Watts	10uW	63uW	36uW	152uW	660uW
Rank	1	3	2	4	5

PSoC Blocks

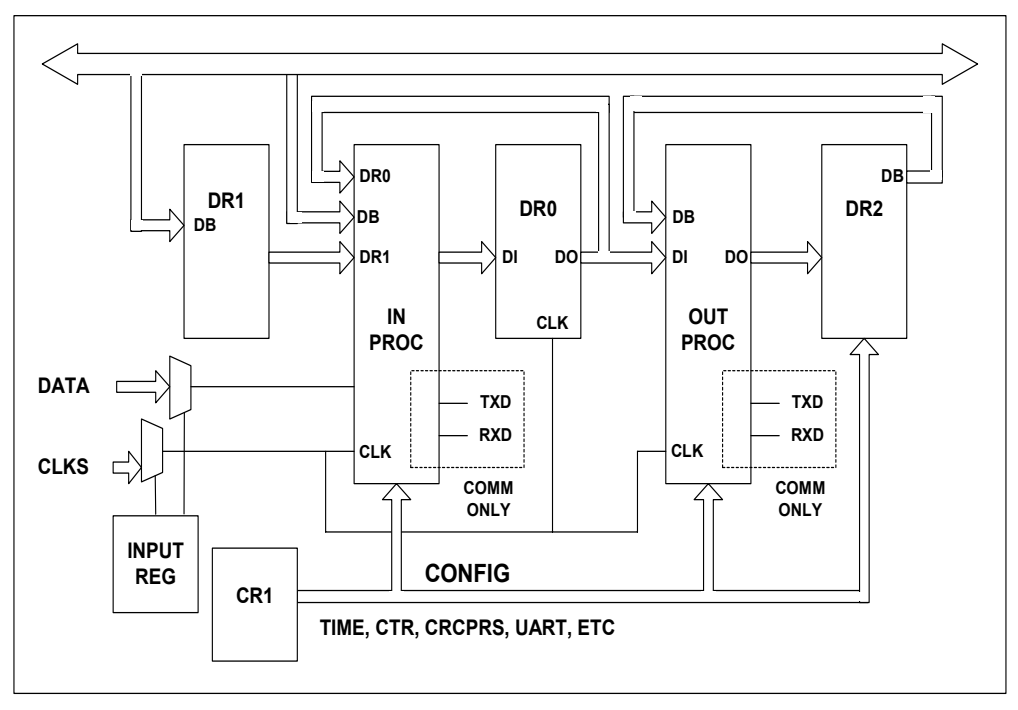


Digital PSoC Blocks

Eight 8-bit Digital PSoC Blocks Available

Two Types:

- Basic (4)
- Communications (4)



- Programmed at the Functional Level
- Not Programmed at the Gate Level

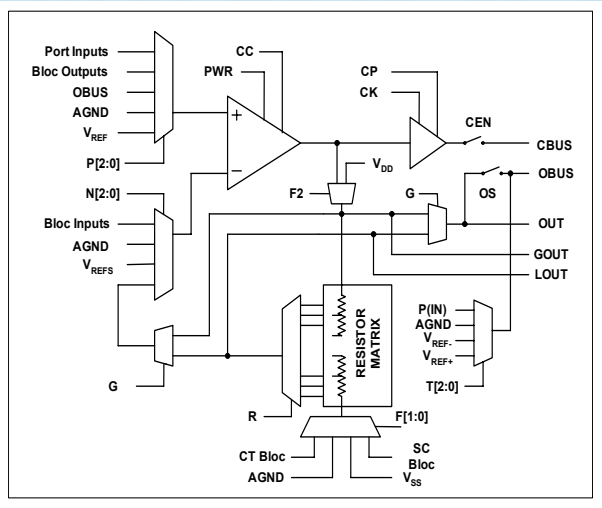
Analog PSoC Blocks

Twelve Analog PSoC Blocks Available

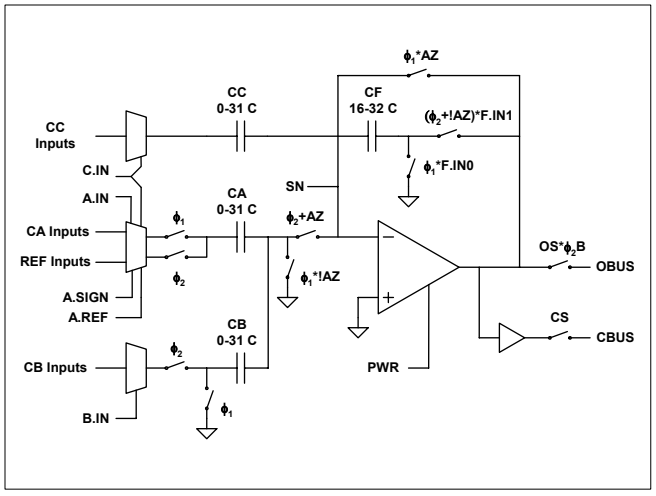
Three Types:

- Continuous Time (4)
- Switch Capacitor C (4)
- Switch Capacitor D (4)

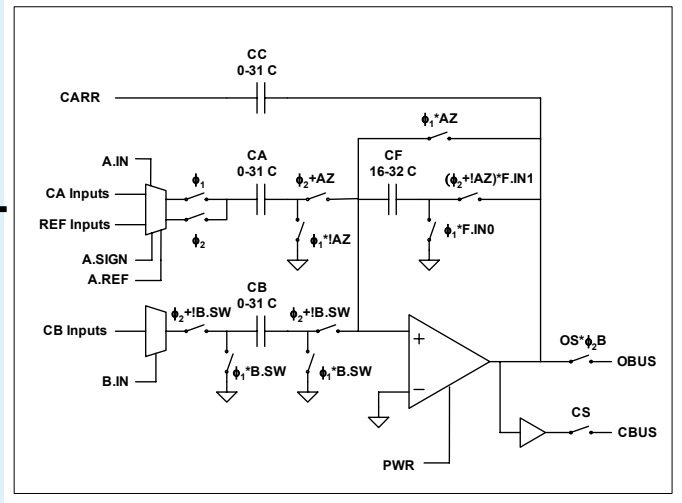
Continuous Time



Switched Capacitor C



Switched Capacitor D



PERSONAL ACCESS ENTERPRISE METRO CORE

User Modules

Pre-configured and Pre-characterized Digital and Analog PSoC Blocks

Analogous to On-chip Peripherals

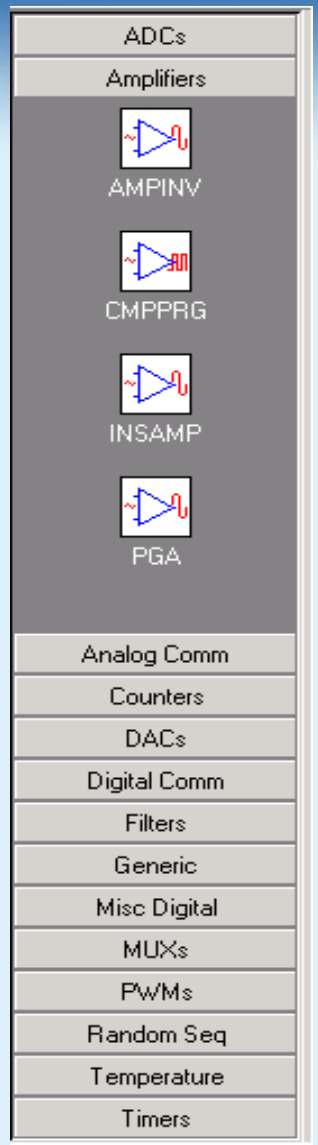
- Timer- Counters – PWM's
- UART – SPI
- A/D –DAC's - SAR

Defines the Register Bits for Initial Configuration

Selected via Double Click in IDE

User Modules Include

- Application Programmer Interfaces (APIs)
- Interrupt Service Routines (ISRs)
- Specific UM Data Sheets



Digital User Modules

8, 16, 24, 32-bit Timer
8, 16, 24, 32-bit Counter
8, 16-bit PWM
8, 16-bit Dead Band Generator
- (2 Phase Underlapped Clock)

Pseudo Random Source (PRS)
Cyclic Redundancy Check (CRC) Generator

I^2C Master
I^2C Slave
SPI Master
SPI Slave
Full Duplex UART
IrDA receiver and transmitter

Analog User Modules

A/D Converters
- 8-bit Successive Approximation
- 8-bit Delta Sigma
- 11-bit Delta Sigma
- 12-bit Incremental
- 7-13 bit Variable Incremental
- Dual input 7-13 bit Variable Incremental
- Tri input 7-13 bit Variable Incremental

D/A Converters
- 6, 8, and 9-bit
- 6 and 8 bit multiplying

Filters
- 2-pole Low-pass filter
- 2-pole Band-pass filter

Amplifiers
- Programmable Gain Amplifier
- Instrumentation Amplifier
- Inverting Amplifier

Programmable Threshold Comparator

DTMF Dialer

Software User Modules

I²C Master

EEPROM

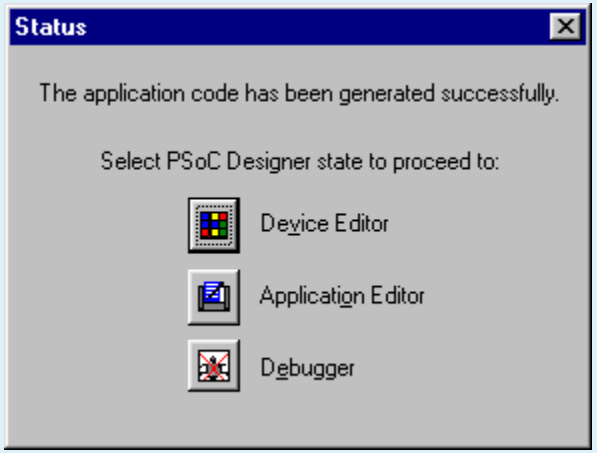
LCD – Interface for Hitachi HD44780 controller

Integrated Development Environment

- Device Editor
- Application Editor
- C Compiler
- Assembler
- Librarian
- Debugger

Device Editor – The End Result

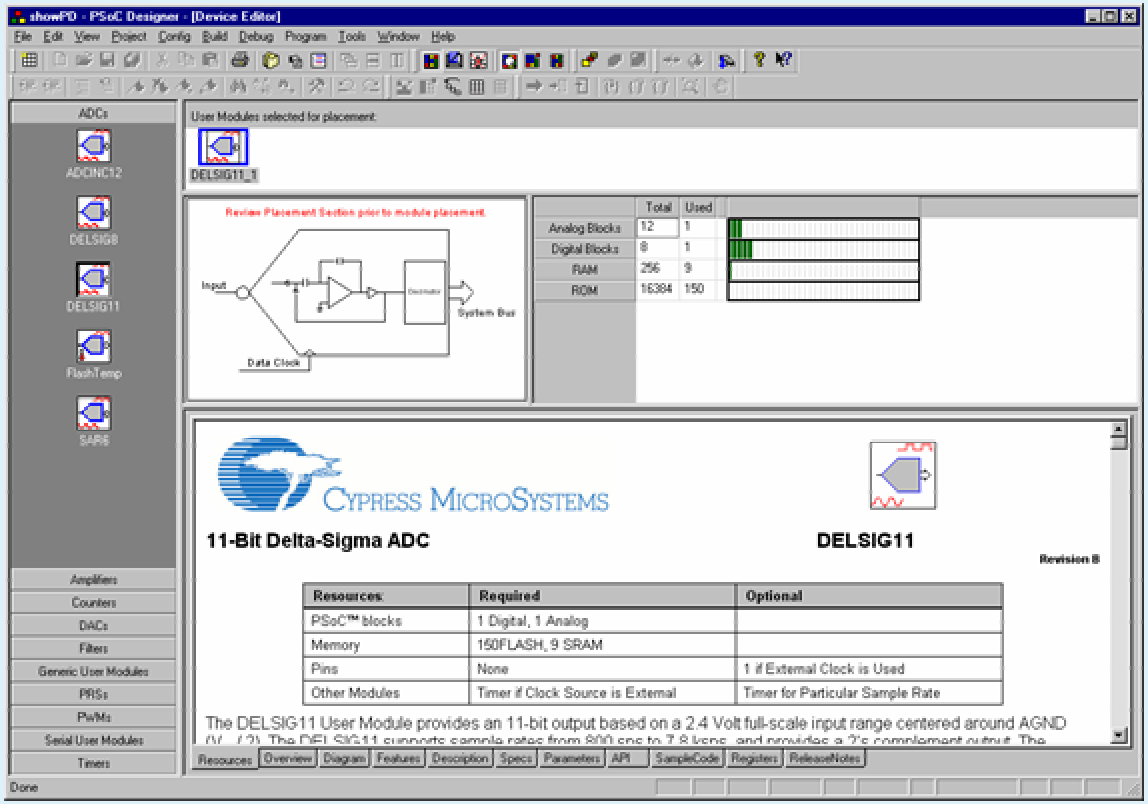
User Clicks “Generate Application” Icon The Software Takes All User Inputs;



- Generates files specifying the configured device
- Sets up the source files for the project application code
- Allows the user to start coding using the Application Editor
- Creates a custom configuration sheet based on your inputs – Your custom “data sheet”

PSoC Designer
Device Editor – Selection Mode

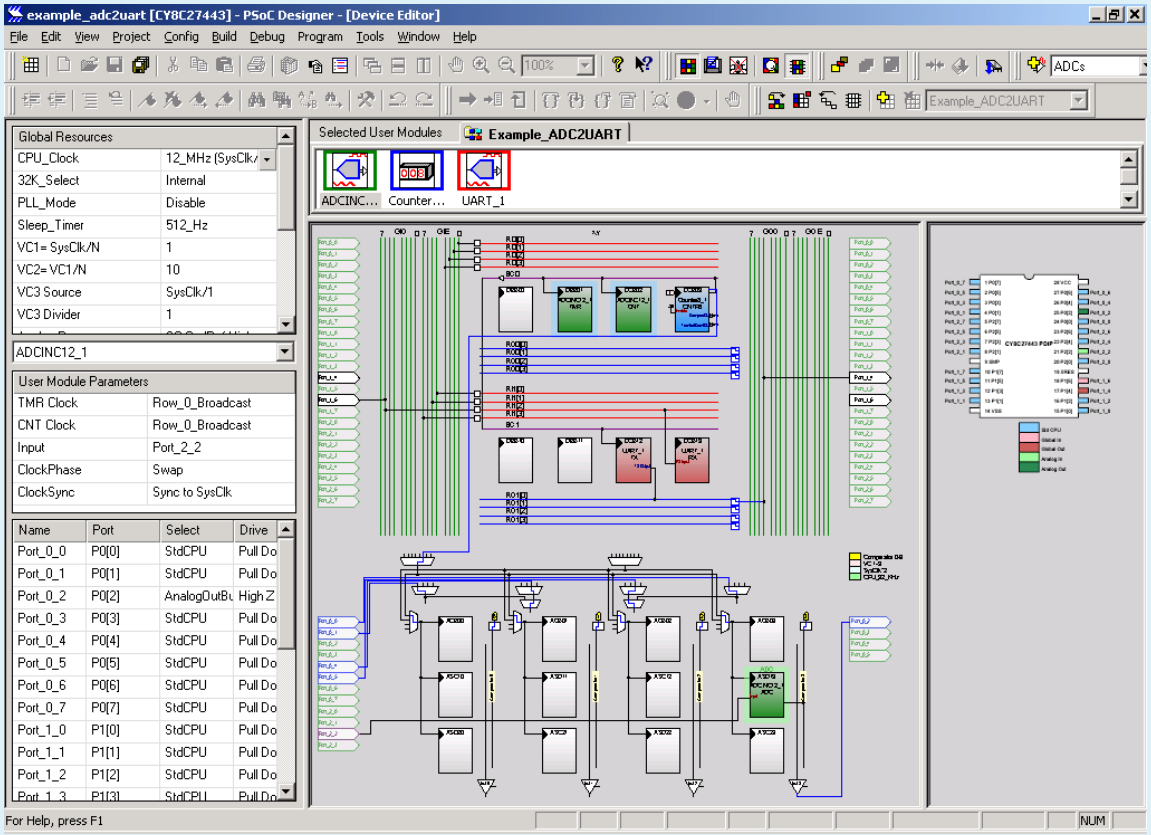
Selecting User Modules



- View Lists of User Modules in catalog
- View datasheet for each user module
- Select user modules and include in current project
- View a running total of available and consumed resources

PSoC Designer
Device Editor – Combined Place & Pinout View

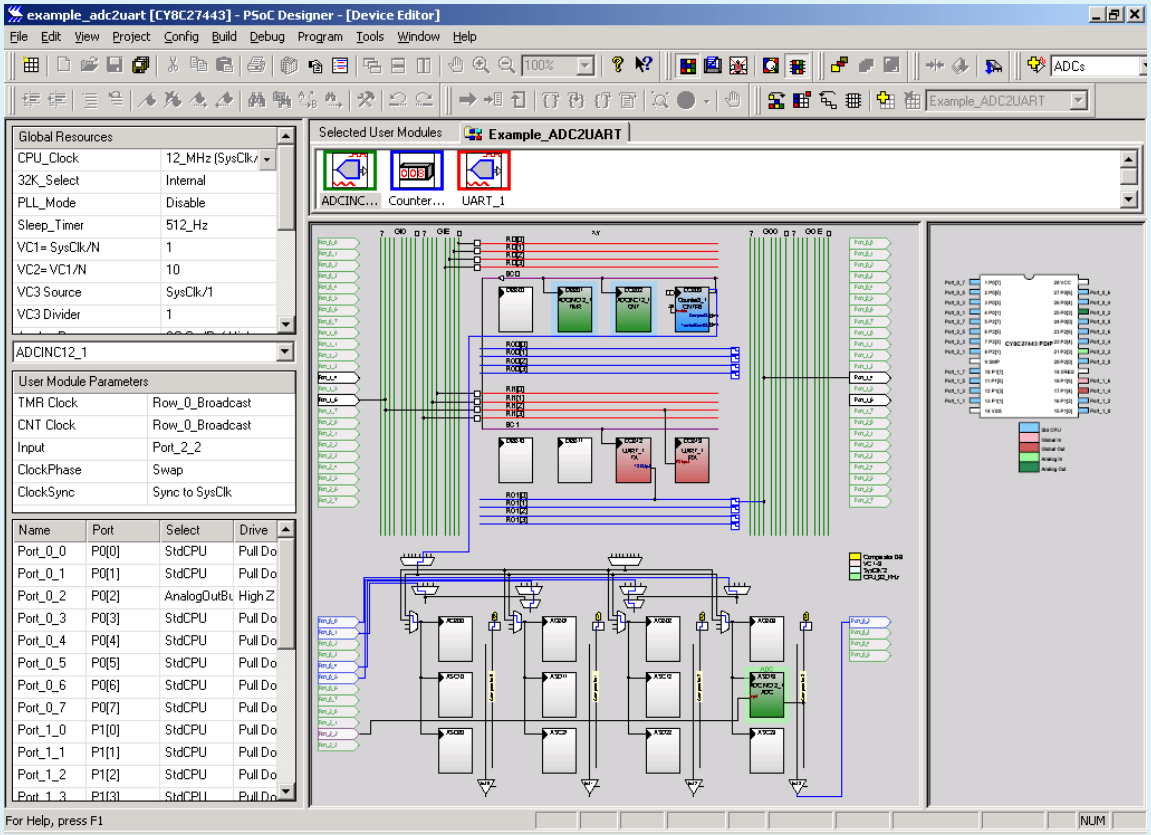
Placing User Modules



- View Block architecture with combined UM & port views
- Generates routed block to block schematic
- Routed global I/O connection schematic
- Step through potential UM placement options
- Select desired placement option for UM
- Select UM and resource interconnections
- Select/configure UM and global device resources
- Define clocking for UMs

PSoC Designer
Device Editor – Combined Place & Pinout View

Specifying Pinout



- View the pin options for the chosen part
- Make connections from pins into User Modules
- Make connections from User Modules out to pins
- Select UM and resource interconnections
- Set the mode and drive level for GPIO pins

PSoC Designer
Device Editor – View Options

Three View Option Methods in Device Editor, Interconnect view

1. View Toolbar

2. View Hotkeys

Zoom In	Ctrl+Click
Zoom Out	Shift+Ctrl+Click
Original View	

3. Menu

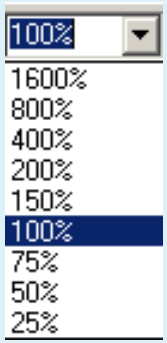
PSoC Designer
Device Editor – View Options

View Toolbar

Original View
- Clicking on the home button restores original view

Pan
- Left click on Pan button to enable or disable pan

Zoom
- Left click on Zoom Button to zoom in/out
- Pull down percentage or type directly into pull down



PSoC Designer
Device Editor – View Options

View Hotkeys

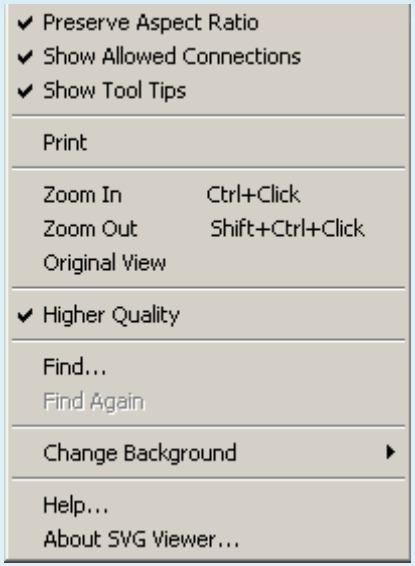
Control + left click
- Holding down control enables zoom in
- Control + shift enables zoom out

Alt + left click
- Holding down alt enables pan
- Alt + shift enables pan up/down or left/right

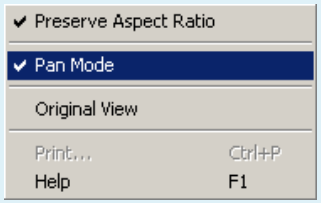
PSoC Designer
Device Editor – View Options

Menu

Right click on empty space for help menu; choose Zoom In, Zoom Out, Original View

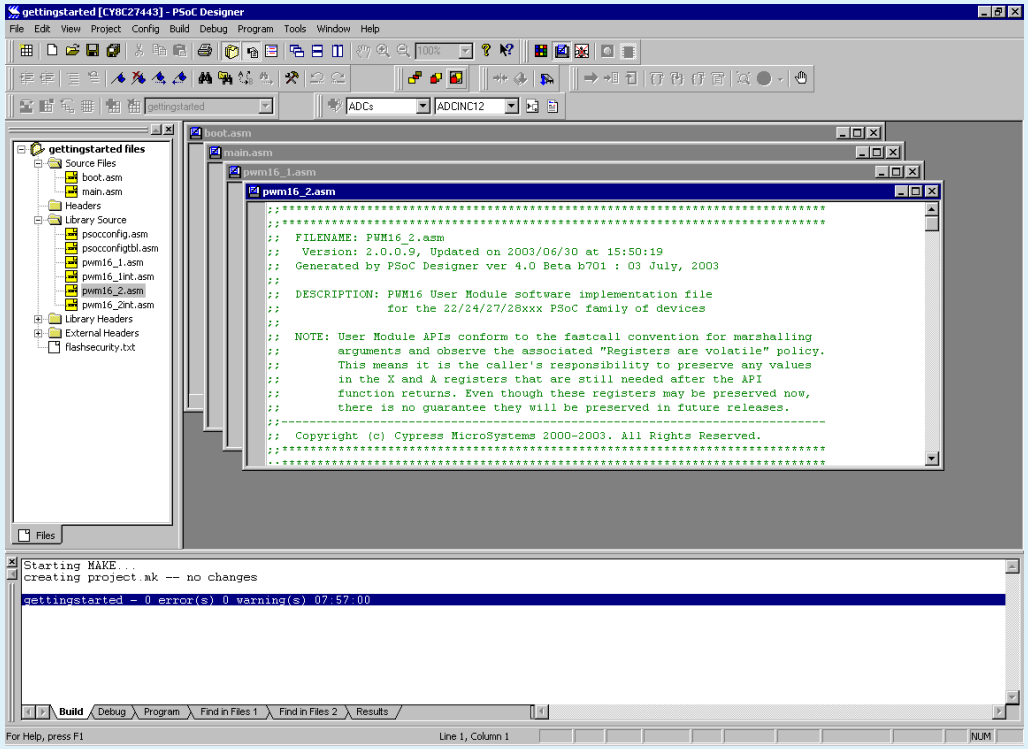


Right click when Pan is enabled to disenable



PSoC Designer
Application Editor

For Users to Write Code
For Users to Assemble/Compile Code



- View and edit individual source files
- Set and remove bookmarks (Editing tool)
- Assemble/compile individual files
- Build entire project including assemble/compile* all files in project
- Source line error pointer

*The C compiler needs to be enabled for use.

PERSONAL ACCESS ENTERPRISE METRO CORE

PSoC Designer C Compiler

The CY3202-C compiler is an optional component of the PSoC Designer IDE. Once enabled, it is fully integrated into the IDE and allows PSoC Designer to support C source level debugging.

Features Include:

- ANSI C Compiler
- Supports Inline Assembly and can Interface with Assembly Modules
- Integrated code compressor
- Modern Stack-Based Architecture
- 7 Basic Data Types Including IEEE 32-Bit Floating Point
- Assembler and Linker
- Math and String Libraries
- C Interrupt Service Routines
- Librarian

PSoC Designer C Compiler

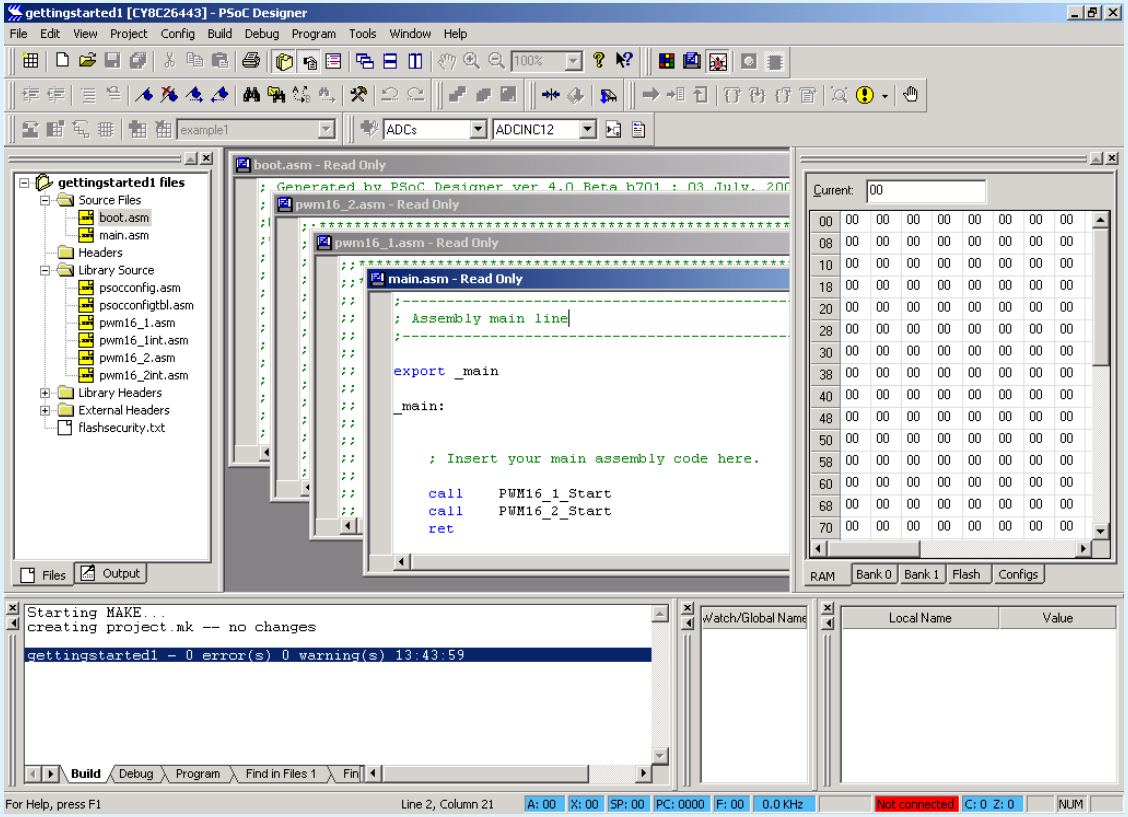
C Interrupts are Supported

#pragma interrupt_handler <name> *

- `reti` is used instead of `ret` to return from the function
- Virtual registers used by the function are automatically saved and restored
- If another function is called from the interrupt handler all virtual registers are saved and restored

Additional Information Available in the C Language Compiler User Guide

Debugger



- Interface to ICE
- View contents of Register and Memory spaces
- Change the contents of the register banks and the RAM
- Run/Halt /Single Step
- Set breakpoints and event points
- Capture trace

PSoC Designer 4.0
Other Features

- Design Rule Checker
  - Global Parameters
  - User Module configuration
- Code Size Reduction
  - Option to link only those API functions that are used
  - C Code Compression by 2% to 10%
- Supports selective build for multiple configurations
- Device floor planner GUI allows selection, placement, and routing of User Modules within a single view
- Debugger Enhancements
  - Single-step mixed C and Assembly
  - View Array Watch Variables

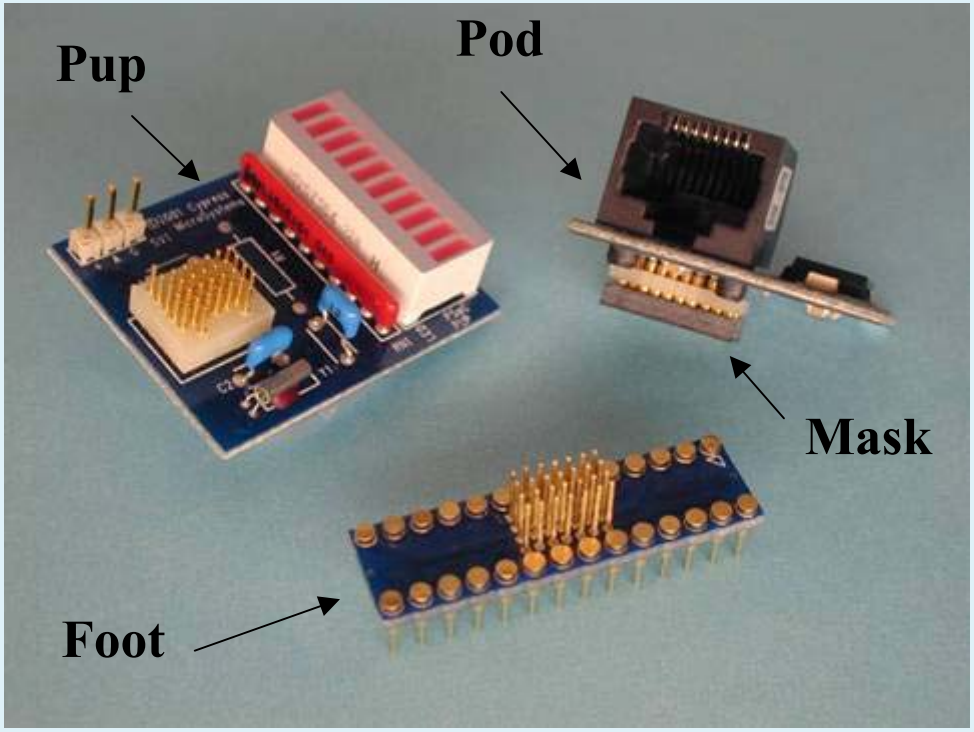
Development Kit

CY3205-DK

Development Kit

Kit includes everything to support the 28-pin PDIP package

PSoC ICE Pod Kits



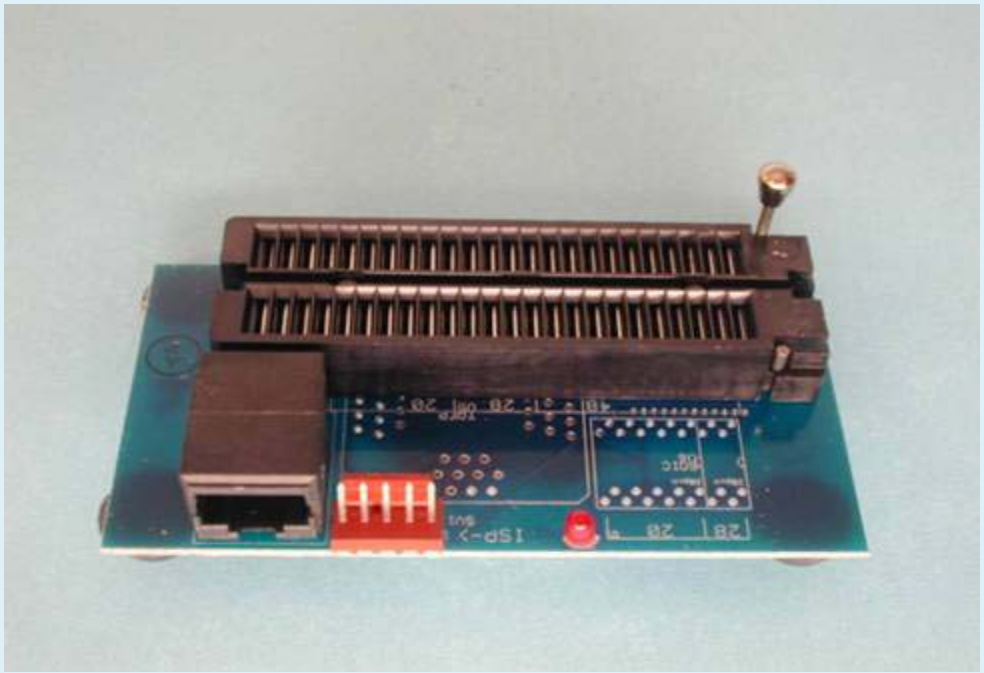
- Smallest POD on the market
- Versions are available for all device/package types
- Sold separately to support various pin-outs
- Every part type/package type has a pod/foot

PSoC ICE Pod Kits

Chip Part #	Pod Kit Part #	Package Type	Feet/Masks	Y-Programmer
CY8C27143-24PI CY8C27243-24PI CY8C27443-24PI CY8C27643-24PI	CY3207-PI	8, 20, 28, 48 PDIP	included	included
CY8C27243-24PVI CY8C27443-24PVI CY8C27643-24PVI	CY3207-PVI	20, 28, 48 SSOP	included	included
CY8C27543-24AI	CY3207-AI	44 TQFP	included	included
CY8C27643-24LFI	CY3207-LFI	48 MLF	included	included
--	CY3207-POD	--	included	--

What is a Y-Programmer???

- Programmer board with socket is available for each package type
- Connects to the ICE in place of the Pod



Y-Programmer

Chip Part #	Spares Kit Part #	Description
CY8C27143-24PI	CY3207-012	2 Spare Pod Feet for 8-Pin DIP
CY8C27243-24SI	CY3207-050	10 Spare Pod Feet for 20-Pin SOIC
CY8C27243-24PVI	CY3207-060	10 Spare Pod Feet for 20-Pin SSOP
CY8C27443-24PI	CY3207-032	2 Spare Pod Feet for 28-Pin DIP
CY8C27443-24SI	CY3207-070	10 Spare Pod Feet for 28-Pin SOIC
CY8C27443-24PVI	CY3207-080	10 Spare Pod Feet for 28-Pin SSOP
CY8C27643-24PVI	CY3207-095	5 Spare Pod Feet for 48-Pin SSOP
CY8C27543-24AI	CY3207-105	5 Spare Pod Feet for 44-Pin TQFP
CY8C27643-24LFI	CY3207-122	2 Spare Pod Feet for 44-Pin MLF

ISSP Programmer

PSoC CY3207ISSP In-System Serial Programmer (ISSP™)

Robust programmer for manufacturing environments.

The ISSP programs a single PSoC IC in one of three ways:

1) mounted on your PCB
2) inserted in the socket included on the ISSP Programmer
3) through a test fixture

Third-party programmers are also available.

PSoC Design Flow

- Determine system requirements
- Choose User Modules
- Place User Modules
- Set global and User Module parameters
- Define the pin-out for the device
- Generate the application
- Review generated code
- Demonstrate working configuration

Our Project Requirements

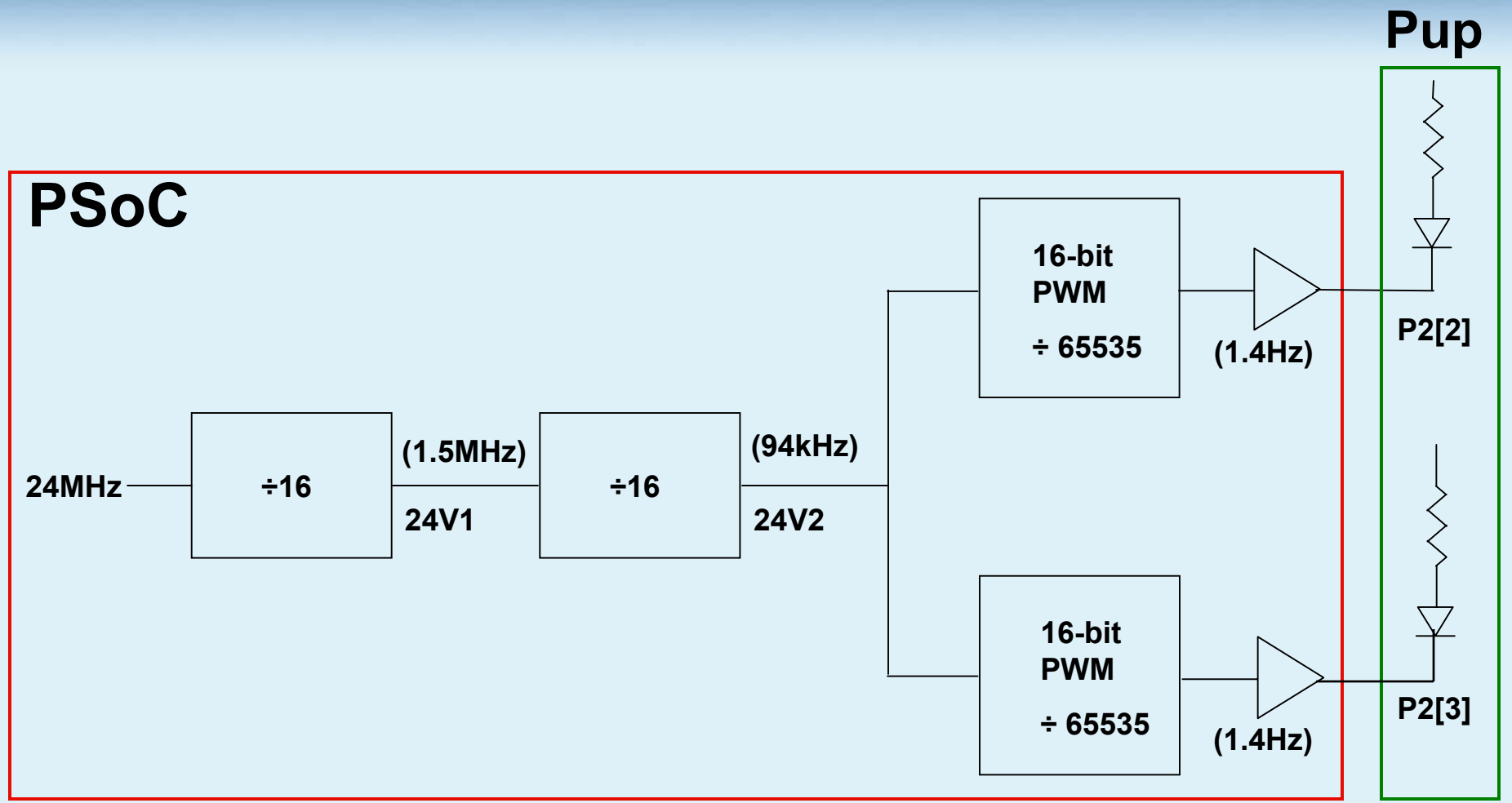
Blink two LEDs at approximately 2Hz, with duty cycle of 40% and 20%

Implementation:

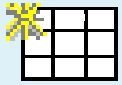
Create An MCU with Two Pulse Width Modulators:

- **Select Two PWM User Modules**
- **Set the PWM parameters**
- **Initialize the global clocks**
- **Connect the PWM outputs to the PSoC Pup LEDs**

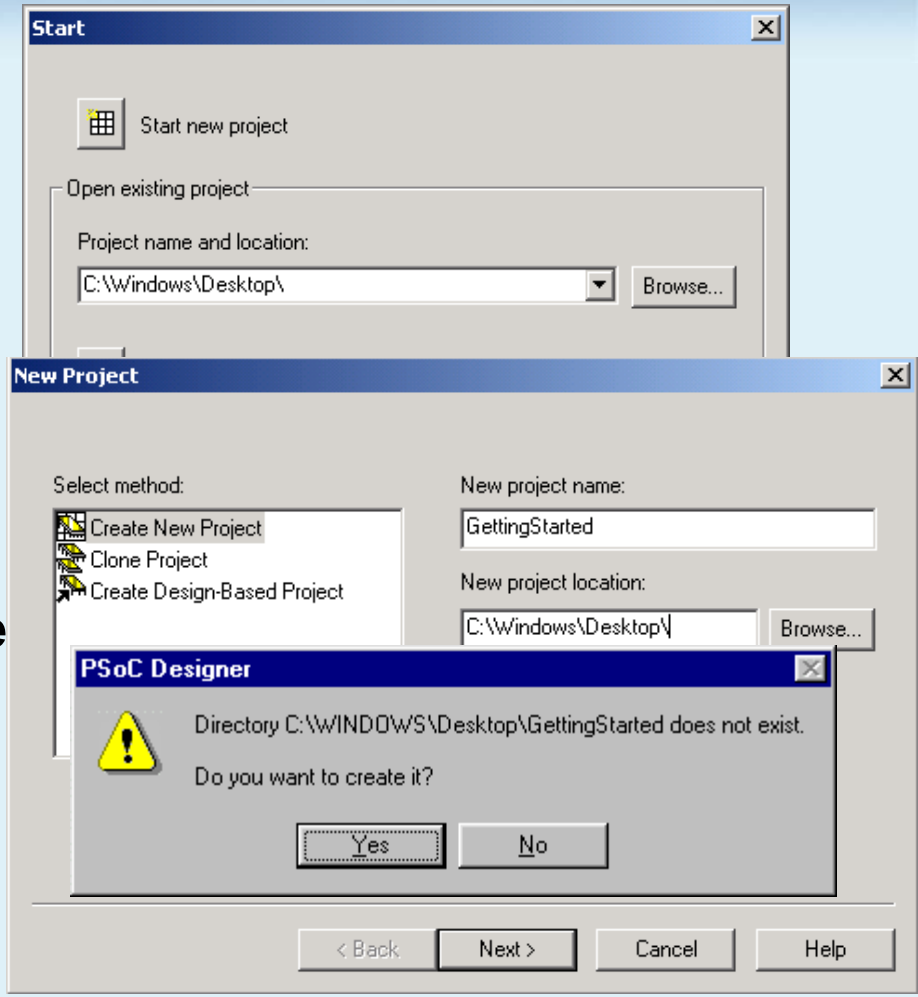
Our Project Implementation



Let's Create Our Project



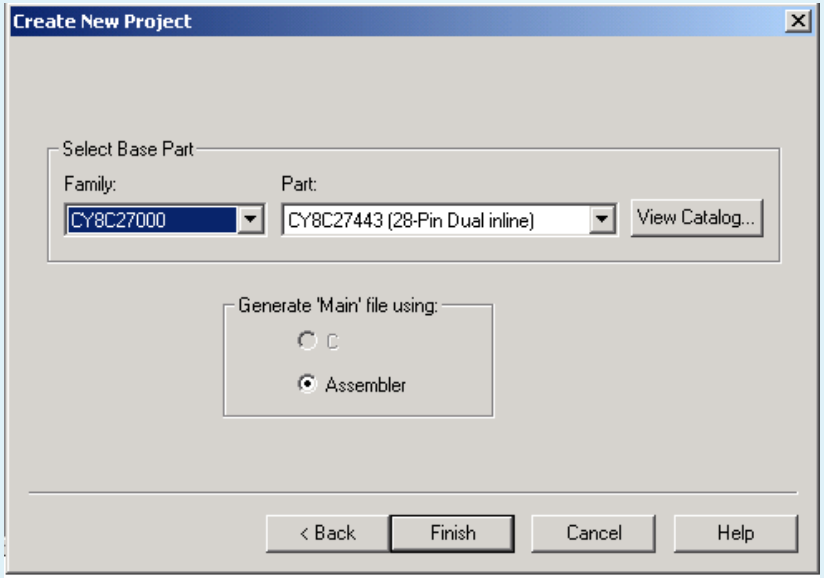
Start PSoC Designer
Click Start new project
Select Create New Project
Type in the name GettingStarted
- Set destination directory
  Desktop/default or select one

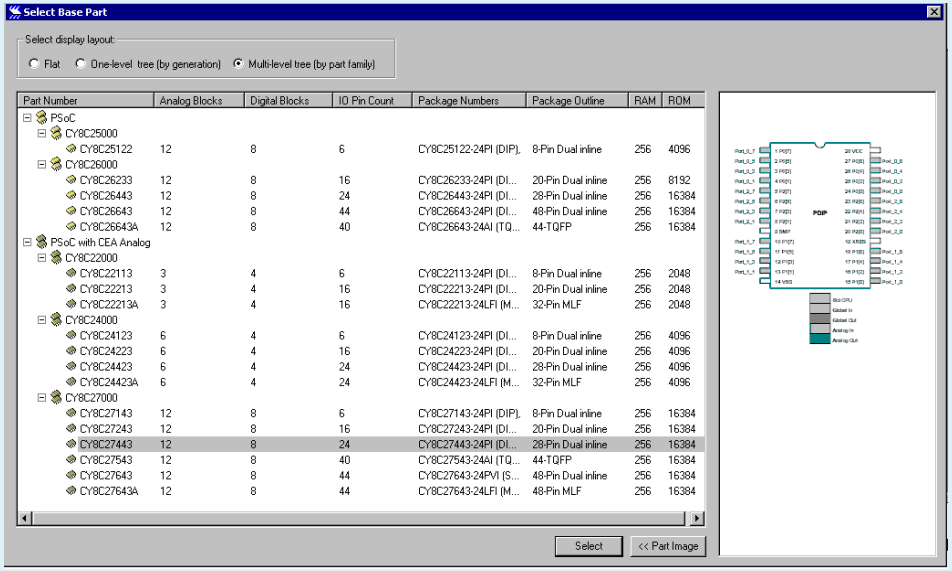


Let's Create Our Project

Select the Base Part

- We'll use CY8C27443 28-Pin
- View the drop-down menu and the parts catalog

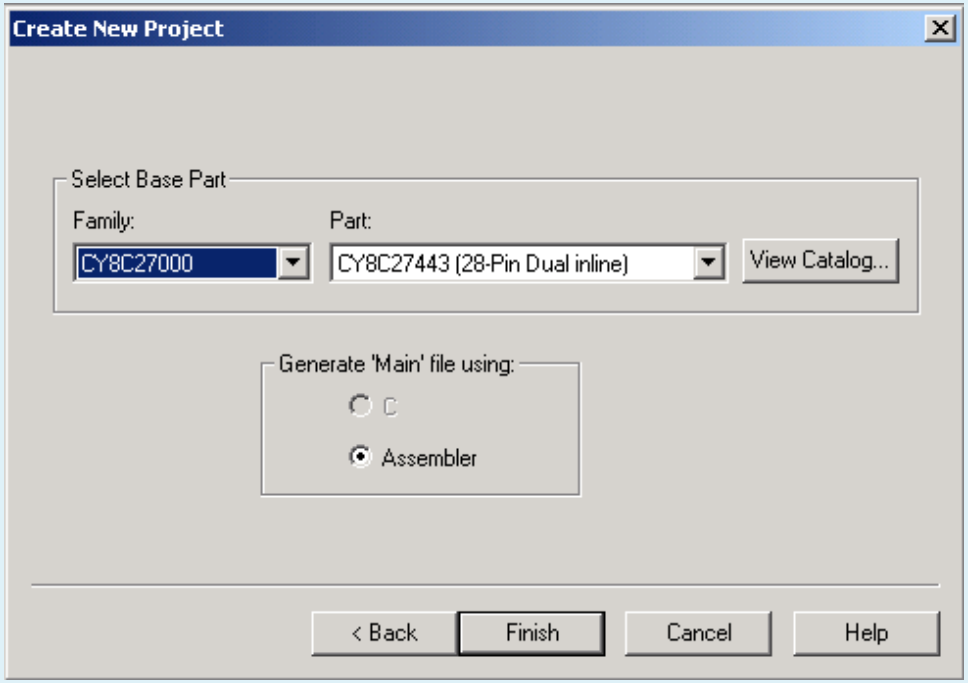




Let's Create Our Project

Select Project's Language

- Assembly and C languages available, (C, only if enabled)
- We'll choose Assembly



Select User Modules

Explore the “Select” Mode of Device Editor

- User Module Catalog (tabs on left side of screen)
- Resource Manager (right side of screen)
- User Module Data Sheet Viewer (bottom middle of screen)
- Adding/Deleting User Module Instances

Select User Modules for this Project

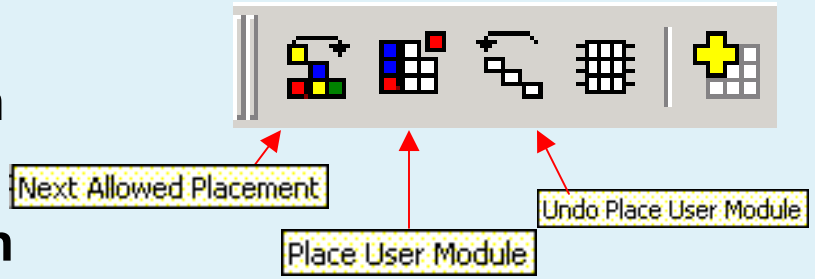
Go to the indicated tab section and double-click

- PWMs tab, PWM16 : A 16-bit Pulse Width Modulator
- Repeat the selection and select a second PWM16

Place User Modules

Explore the "Interconnect View" Mode of Device Editor

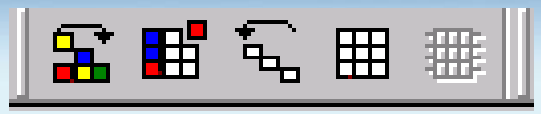
- Select the "Active" UM block
- Next Allowed Placement icon
- Place User Module icon
- Undo Place User Module icon



Place User Modules for this Project

- How do I know where to place the User Modules?
- How does PSoC Designer help me?

Place User Modules



Try-out the modules individually first

- **See how restrictive they are, then return to original location**

PSoC Designer will only allow the modules to be placed where the chip can support them

PSoC Designer will not prevent a placement that may create a conflict for resources

- Example: **If you have an ADC and temperature sensor, they both use the comparator bus. There is only one comparator bus per column, therefore these two UMs must reside in separate columns in order to be used simultaneously.**

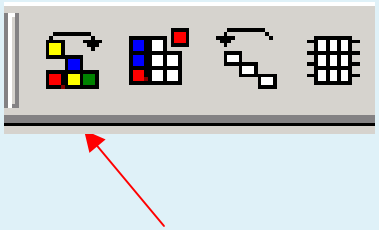
Read the UM Data Sheets for details

Use the Cypress MicroSystems Online Resources

- **www.cypressmicro.com/support**

Place User Modules

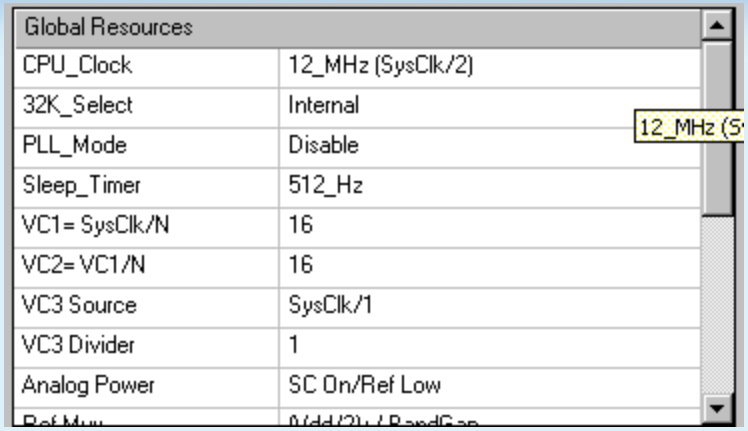
Place the two selected User Modules.



PWM16_1 – Digital Blocks DBB00/DBB01
PWM16_2 – Digital Blocks DBB10/DBB11

Recommend placing the PWM's in the Basic Digital Blocks to Save the Digital Communication Blocks

Configure Global Resources



CPU_Clock: 12MHz

32K_Select: Internal

- **Not using an external crystal**

PLL_MODE: Disable

- **PLL can only be enabled when 32K_Select is External (crystal)**

Sleep_Timer: 512_Hz. (Default)

VC1 = SysClk/N: Set to 16

- **This divides 24MHz by 16 = 1.5MHz**

VC2 = VC1/N: Set to 16

- **This divides the 24V1 by 16 (1.5MHz/16=94kHz)**

VC3 Source: SysClk/1

VC3 Divider: 1

Configure Global Resources

Analog Power: SC On/Ref Low

- This is required to power up any of the analog blocks, depending on the number of analog functions. A Ref Med or Ref High may be required (and will increase power consumption)

Ref Mux: (V_{dd}/2) ±Bandgap (default)

AGndBypass: Disabled

Op-Amp Bias: Low (default)

- This is not recommended as anything but low

A_Buff_Power: Low (default)

- This selects the power level of the analog output buffer
- There is a tradeoff between drive output power and power consumption.
  Low is adequate for most projects

SwitchModePump: OFF

Configure Global Resources

Trip Voltage [LVD (SMP)]: 4.64V (5.0V)

Supply Voltage: 5.0V

SysClk Source: Internal 24_MHz

SysClk*2 Disable: Enable

Configure User Modules

PWM16_1: We want to generate a 1/5 duty cycle

User module parameters can be configured in two ways: through the GUI or through the User Module Parameters window. In this class we will use the User Module Parameters window in the left bottom corner.

- Set Clock to VC2 (94kHz)
- Set Enable High to keep the PWM always running
- Set CompareOut to Row_0_Output_0
- Set TerminalCountOut to None
- Set Period to 65535 (1.4Hz)
- Set PulseWidth to 13107
- Compare Type Less Then Or Equal
- Interrupt Type Terminal Count
- ClockSync to Sync to SysClk
- InvertEnable set to Normal

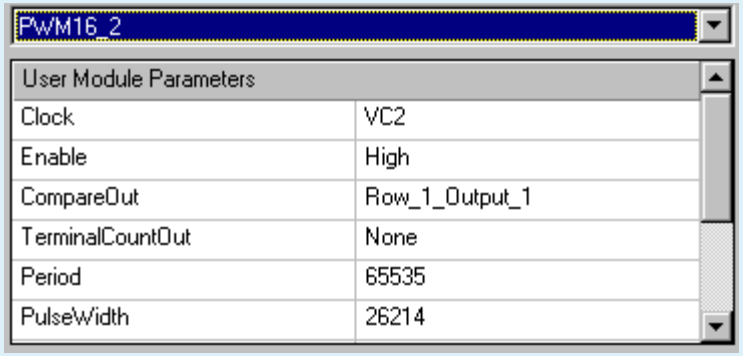
PWM16_1

User Module Parameters	
Clock	VC2
Enable	High
CompareOut	Row_0_Output_0
TerminalCountOut	None
Period	65535
PulseWidth	13107

Configure User Modules

PWM16_2: We want to generate a 2/5 duty cycle

- Set Clock to VC2 (94kHz)
- Set Enable High to keep the PWM always running
- Set CompareOut to Row_1_Output_1
- Set TerminaCountOut to None
- Set Period to 65535 (1.4Hz)
- Set PulseWidth to 26214
- Compare Type Less Then Or Equal
- Interrupt Type Terminal Count
- ClockSync to Sync to SysClk
- InvertEnable set to Normal



Interconnect Blocks to Resources

What interconnection possibilities are there?

- **Data Inputs**
- **Data Outputs**
- **Clocks**
- **Block-to-block**

When you specify a PSoC block connection to a pin you are making a physical connection to the hardware of the PSoC device.

Define the Pin-out

What pins need to be defined?

- UM Inputs
- UM Outputs
- General Purpose IO

What happens as pins are defined?

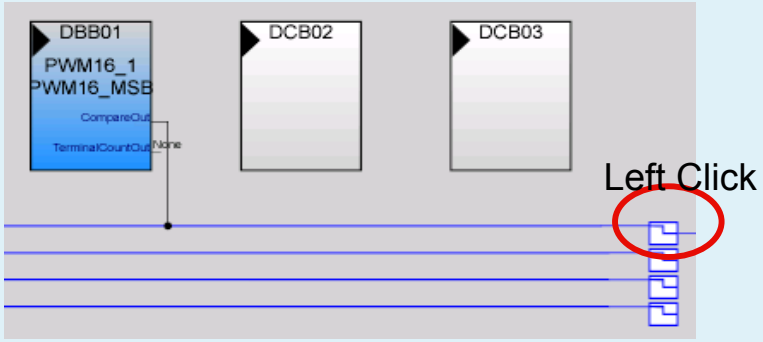
Pin-out our project

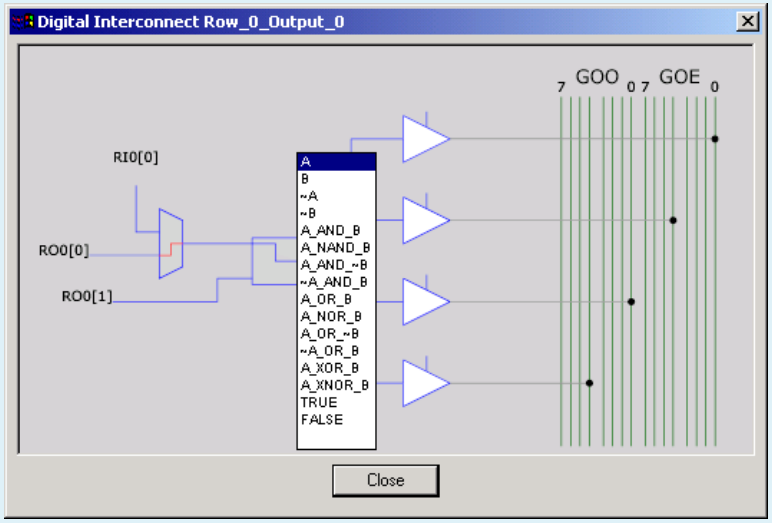
- LEDs

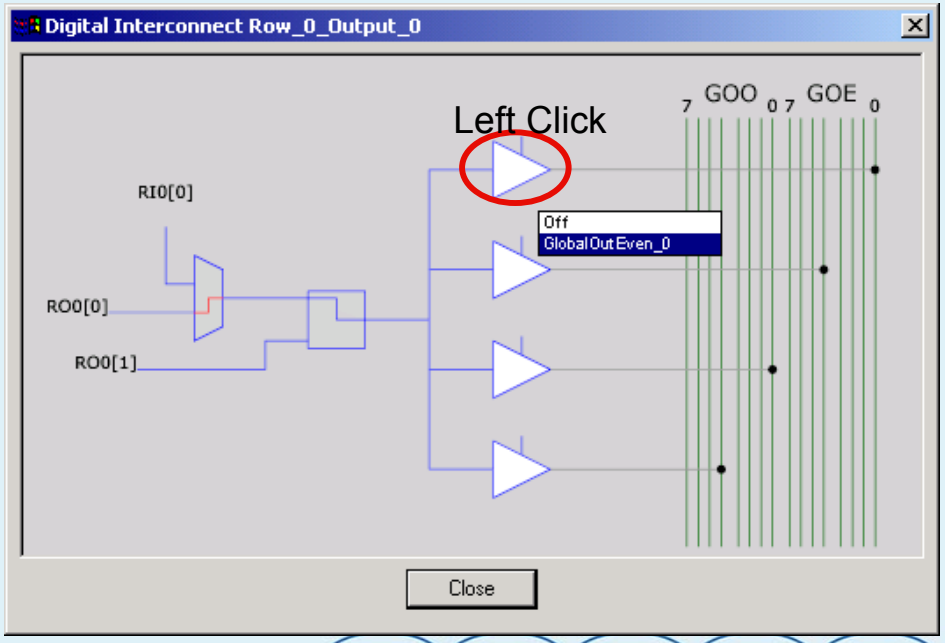
Interconnect Blocks to Resources

Route PWM16_1 to pin:

- **Connect PWM16_1 output to Row_0_Output_0**
- **Connect Row_0_Output_0 to GlobalOutEven_0**



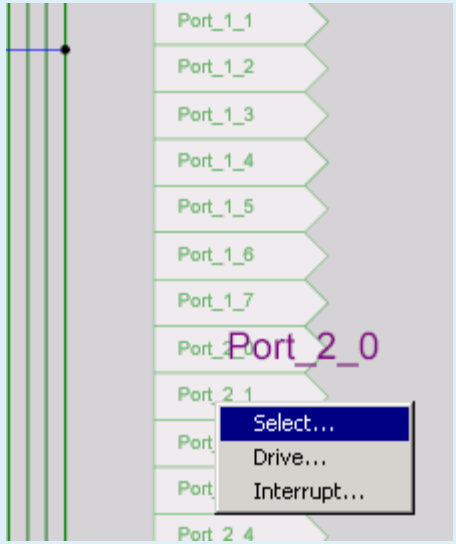


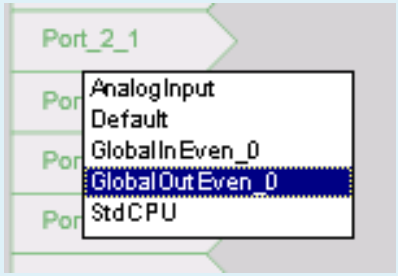


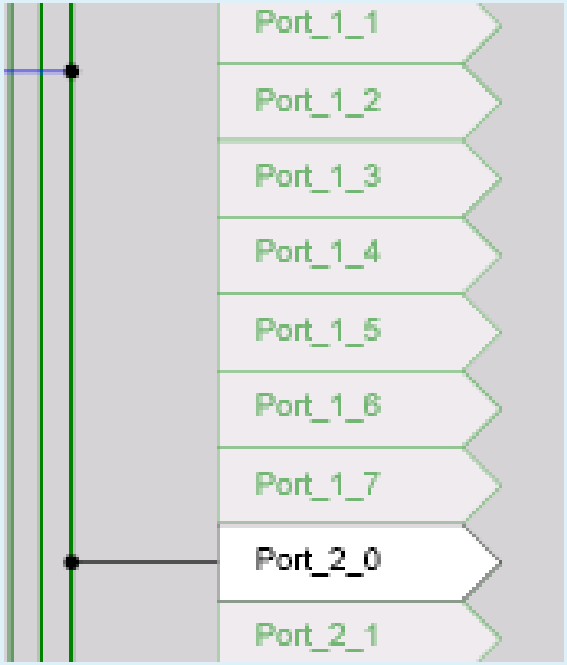
Interconnect Blocks to Resources

Route PWM16_1 output to pin

- **Port 2 is connected to the LEDs on the Pup board**

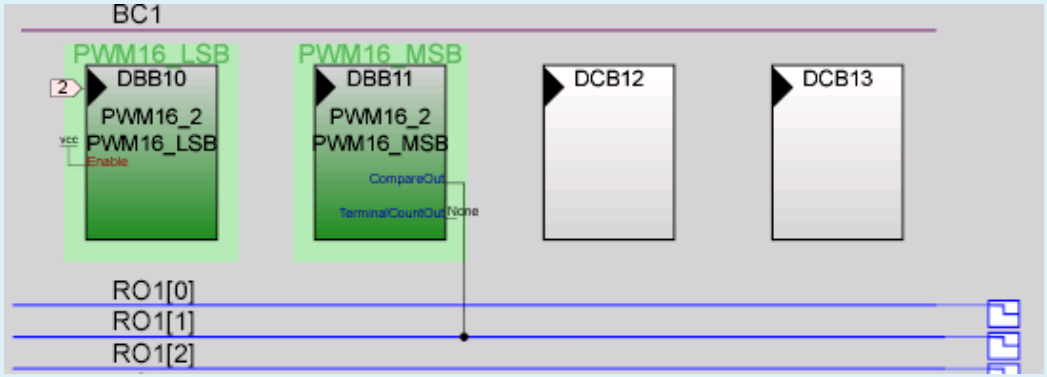


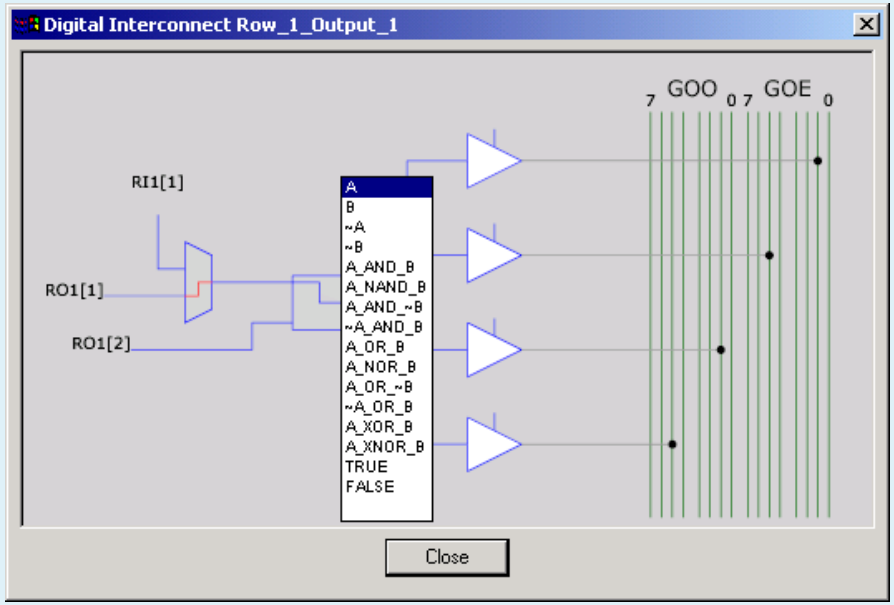


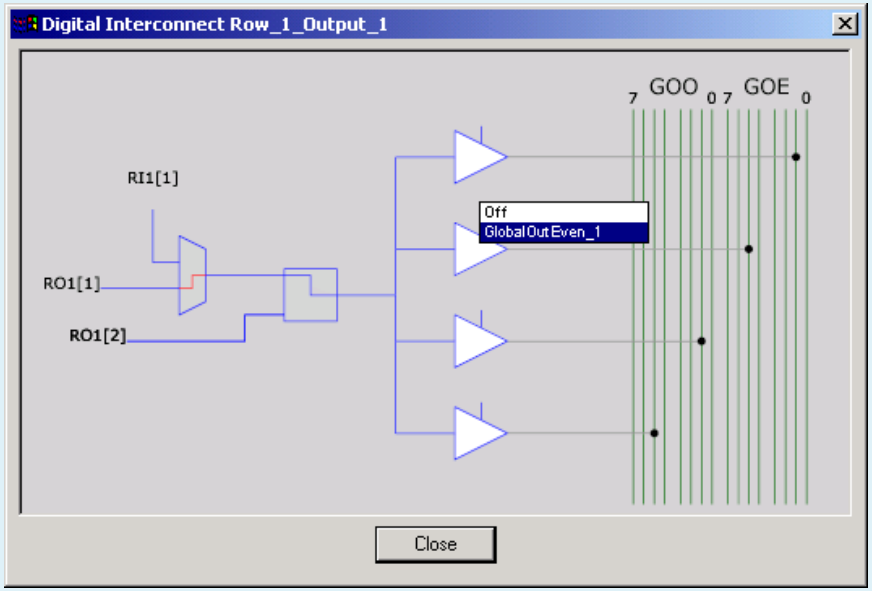


Interconnect Blocks Resources

Route PWM16_2 output to pin

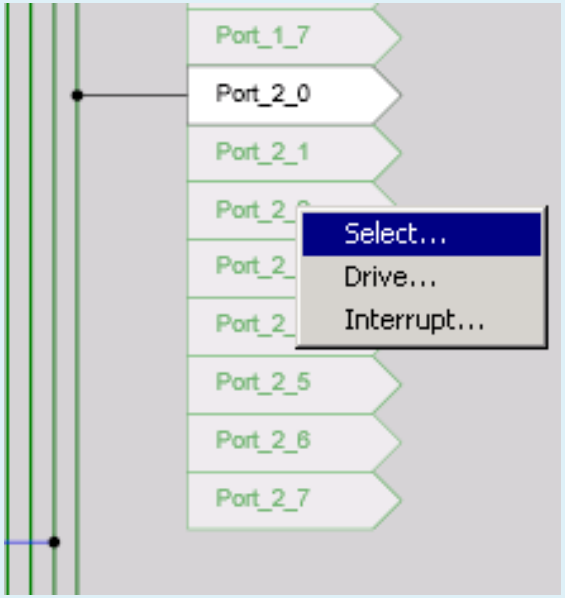


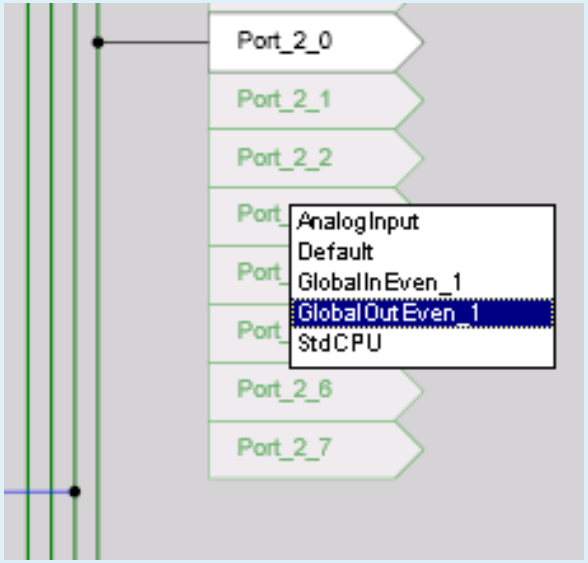


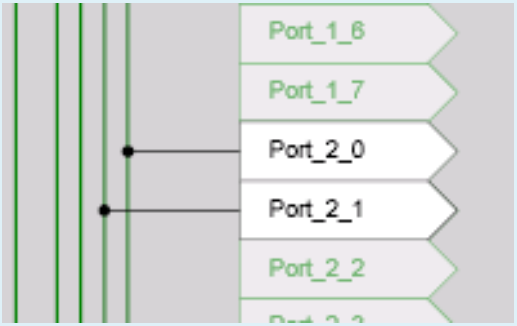


Interconnect Blocks Resources

Route PWM16_2 output to pin

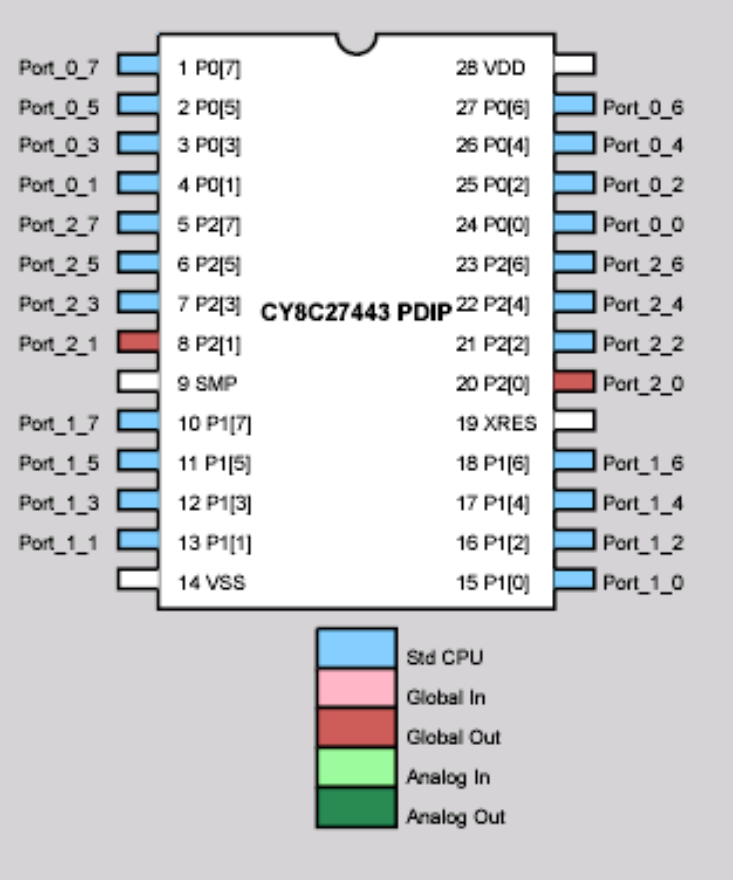




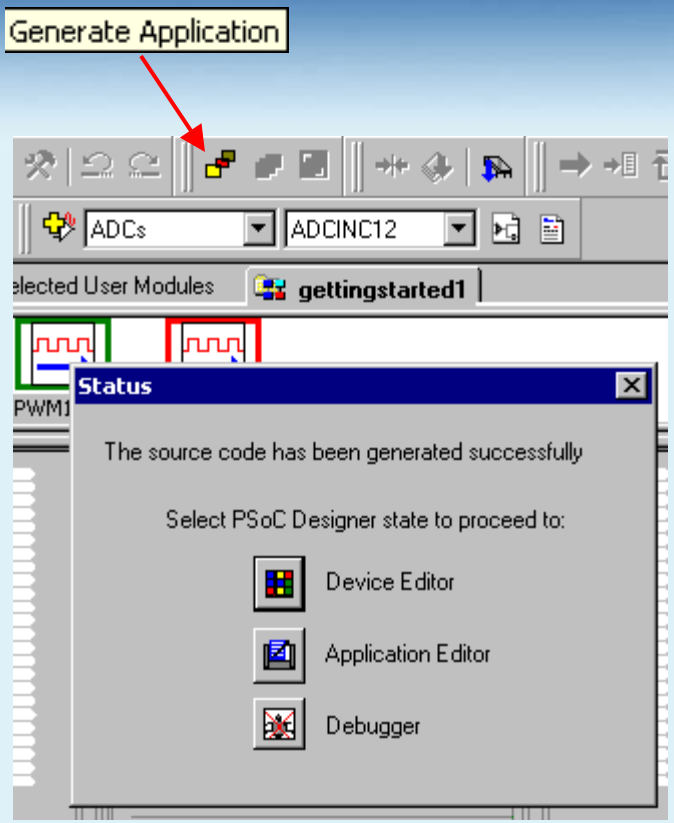


Interconnect Blocks to Resources

Pin layout:



Configuration Complete!



Save project – Go to File tab
Now what? Where are we?

Time to "Generate Application"

- **All settings used by PSoC Designer to create the boot-up code to configure the registers at reset**
- **ISRs are created (but not updated)**
- **APIs are created or updated**
- **Device Data Sheet generated**

You must Generate Application whenever changes are made to the configuration

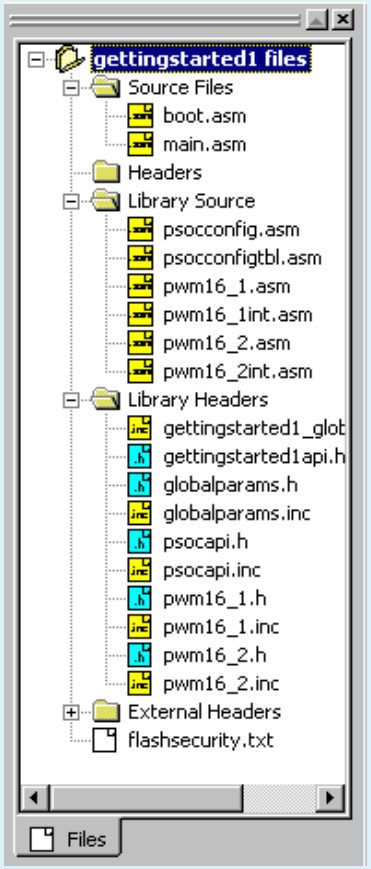
Time to Create Application Code

PSoC Designer generates application code based on the configurations you just defined in the Device Editor.

Project File Tree, located to the left of the application window, contains:

- all interrupt routines
- header files
- include files
- configuration tables

All API's and ISR's can be modified by the user.



Create Application Code

Open the PWM16_1.asm file

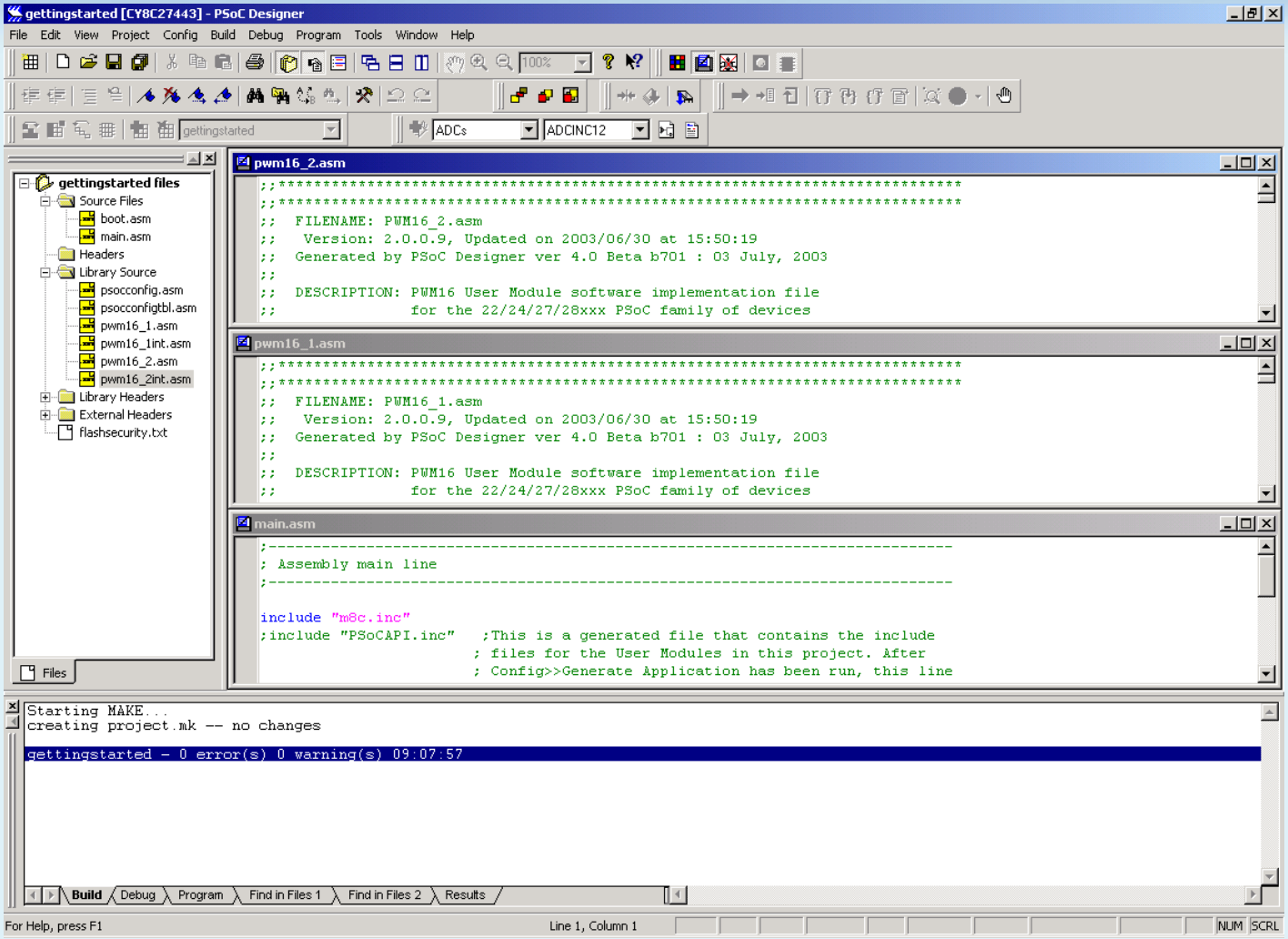
Select the PWM16_1_Start line routine and copy and paste it into the main.asm file

Open the PWM16_2.asm file

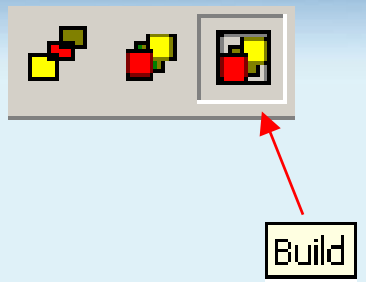
Select the PWM16_2_Start line routine and copy and paste it into the main.asm file

```
export _main

_main:

    ; Insert your main assembly code here.
    call    PWM16_1_Start
    call    PWM16_2_Start

    ret
```

Create Application Code



Build Project



Assembles code, links, and locates

Can individually assemble files as well

Explore Application Editor Features

- Project file management (view/add/delete files)
- Finding compilation errors

Execute Project Within Debugger

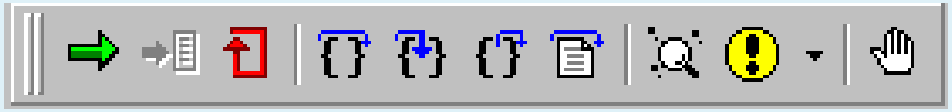
Switch to the Debugger – What's Different?

- Looks like Application Editor, but files are read-only

Connect to the ICE 

Download the project to ICE 

Execute Project Within Debugger

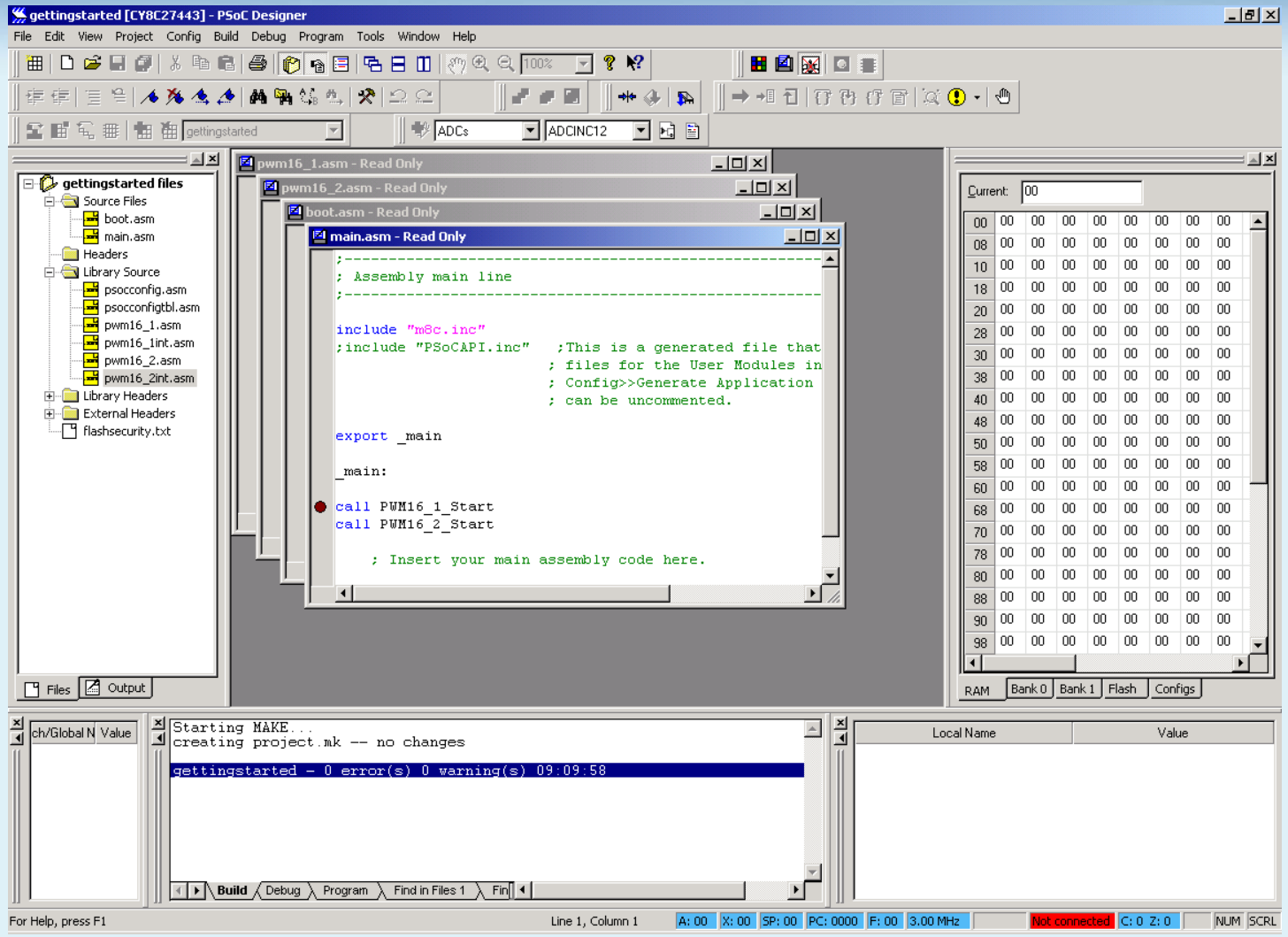


Select the green arrow – Go button

The two LED's should flash at rotating rates

Let's set a breakpoint on the first line of code in the main.asm routine

Execute Project Within Debugger



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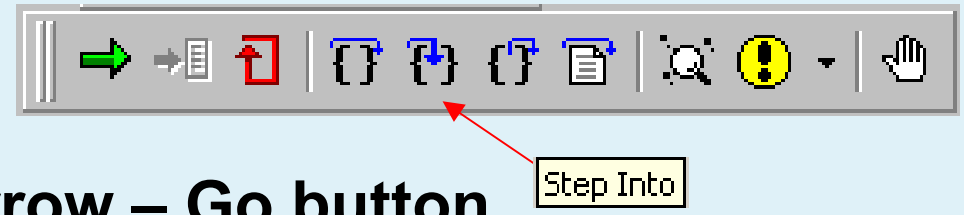
Execute Project Within Debugger



Select the green arrow – Go button

The program will stop at the first call to Start the PWM

Use the Step function (Second blue arrow) to step through the assembly code.

Observe the LED's

Module Objectives

Section 1: Introduce PSoC

Section 2: PSoC Designer IDE Software

- PSoC In-Circuit Emulator (ICE)

Section 3: Hands on Designing a System with PSoC

- Determine system requirements
- Choose User Modules
- Place User Modules
- Set Global and User Module Parameters
- Define the Pin-out for the device
- Generate the application files
- Review generated application code
- Demonstrate Simple Debugging

Section 4: Cypress Microsystems Commitment to Support

Phone Support

Applications Hotline

- Live CMS applications engineer support when you need it

1-800-669-0557 ext 4814

On-line Support

http://www.cypress.com/support/

Self help knowledge base

Submit online applications support with a 4-hour response guarantee

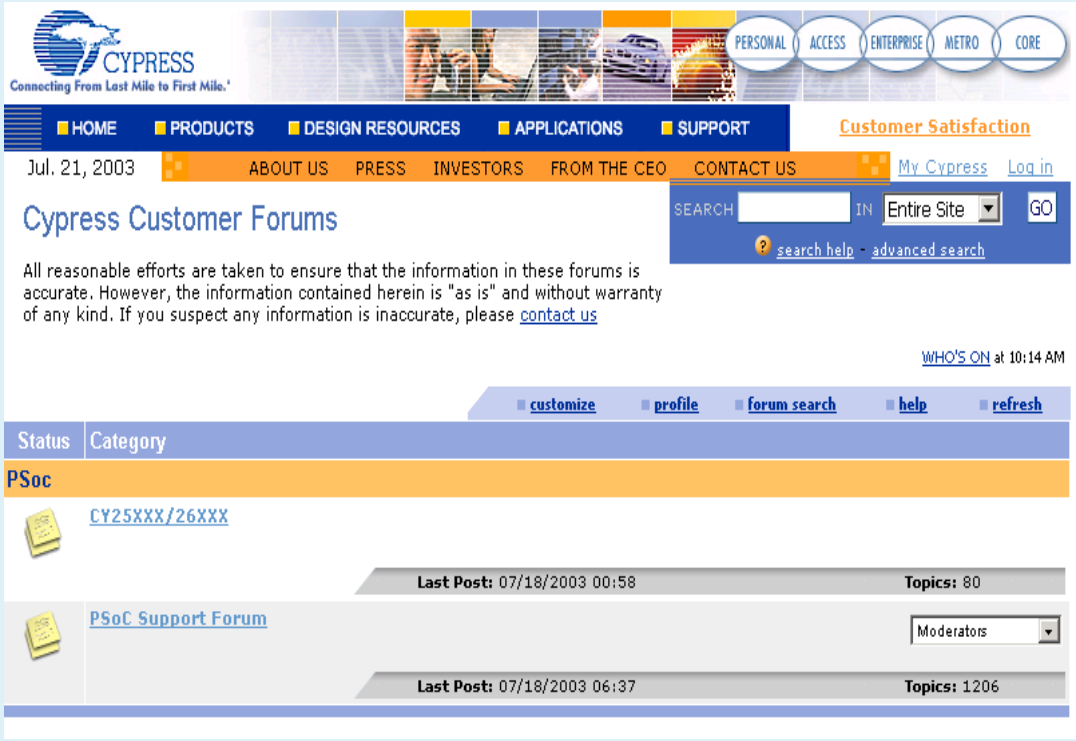
On-line Support

http://www.cypress.com/forums/

User Forums

See solutions to commonly asked questions

Get answers quickly from other PSoC users.



Additional Support Resources

- Application Notes
- Demonstration Designs
- Cypress Field Application Engineers

Tele-Training

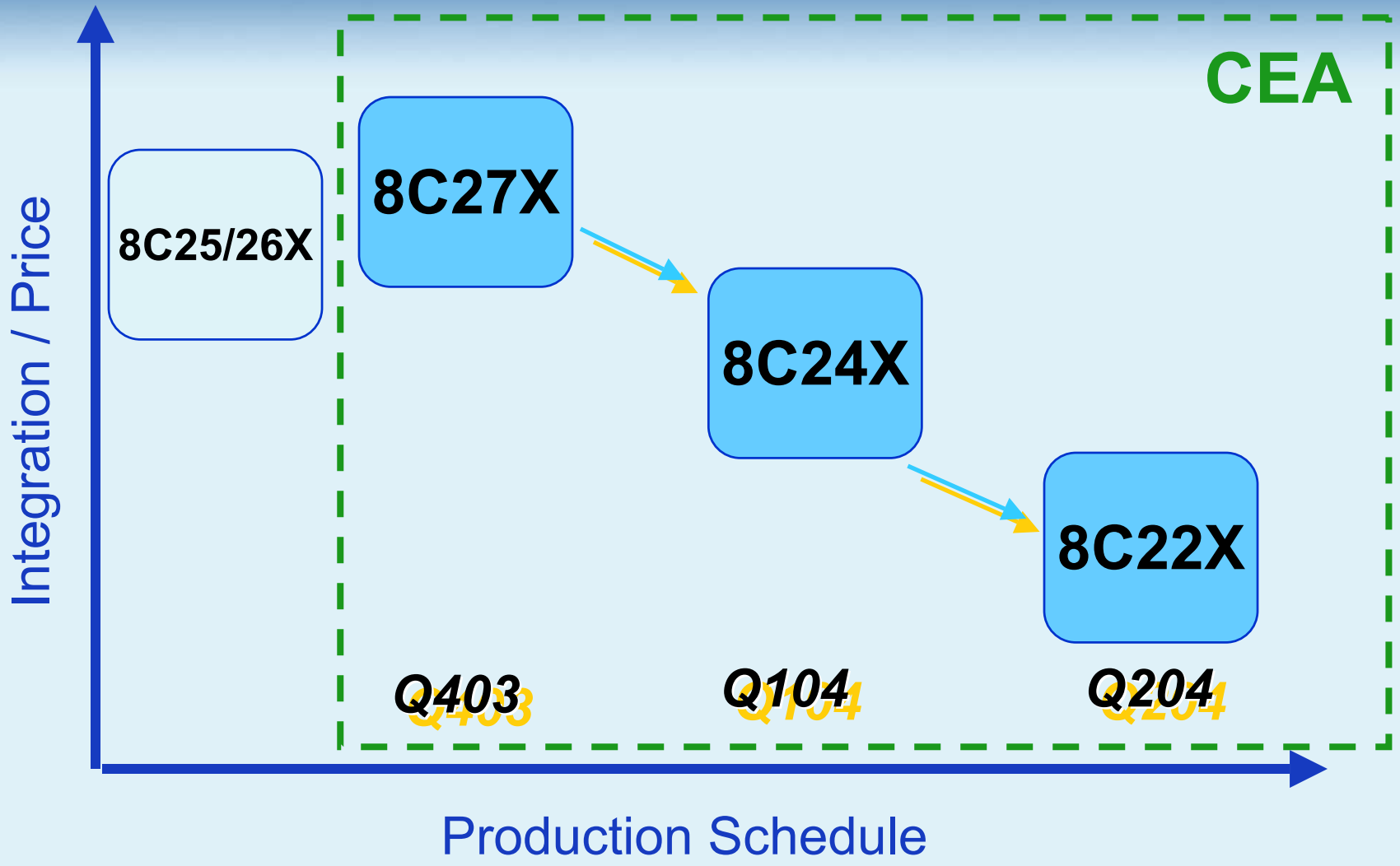
- LIVE Classes Weekly
- Example design project completed during each class
- High quality presentation is available for download
- Taught by factory PSoC experts
- Classes for all levels of experience

Microcontroller Experts Endorse PSoC

- More than 160 design consultants are enrolled in the Cypress MicroSystems program.
- Contact information and short bio on each consultant can be viewed at:

  www.cypress.com/support/cypros.cfm

PSoC Roadmap



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PSoC Roadmap

	Flash Size	Ram Size	Pins	Analog Blocks	Digital Blocks	Hardware I^2C	CEA
8C25/26X	16KB	256	8,20,28,48	12	8	N	N
8C27X	***16KB***	***256***	***8,20,28,48***	***12***	***8***	***Y***	***Y***
8C24X	***4KB***	***256***	***8,20,28***	***6***	***4***	***Y***	***Y***
8C22X	***2KB***	***256***	***8,20***	***3***	***4***	***Y***	***Y***

Product Family

Flexible, *Highly* Integrated SOC, Cost-competitive *Solution*

Marketing Part No.	Flash (Kbytes)	RAM (Bytes)	SMP	Package	Pins
CY8C27143-24PI	16	256	No	DIP	8
CY8C27243-24PVI	16	256	Yes	SSOP	20
CY8C27243-24PVIT	16	256	Yes	SSOP (Tape and Reel)	20
CY8C27443-24PI	16	256	Yes	DIP	28
CY8C27443-24PVI	16	256	Yes	SSOP	28
CY8C27443-24PVIT	16	256	Yes	SSOP (Tape and Reel)	28
CY8C27543-24AI	16	256	Yes	TQFP	44
CY8C27643-24PVI	16	256	Yes	SSOP	48
CY8C27643-24PVIT	16	256	Yes	SSOP (Tape and Reel)	48
CY8C27643-24LFI	16	256	Yes	MLF	48

Congratulations!

Congratulations you have completed a full project using the PSoC™ Mixed Signal Array with onboard controller.

A similar example to this project can be found in the Example folder. (Example_PWM_28pin). The example uses 4 PWM16's.

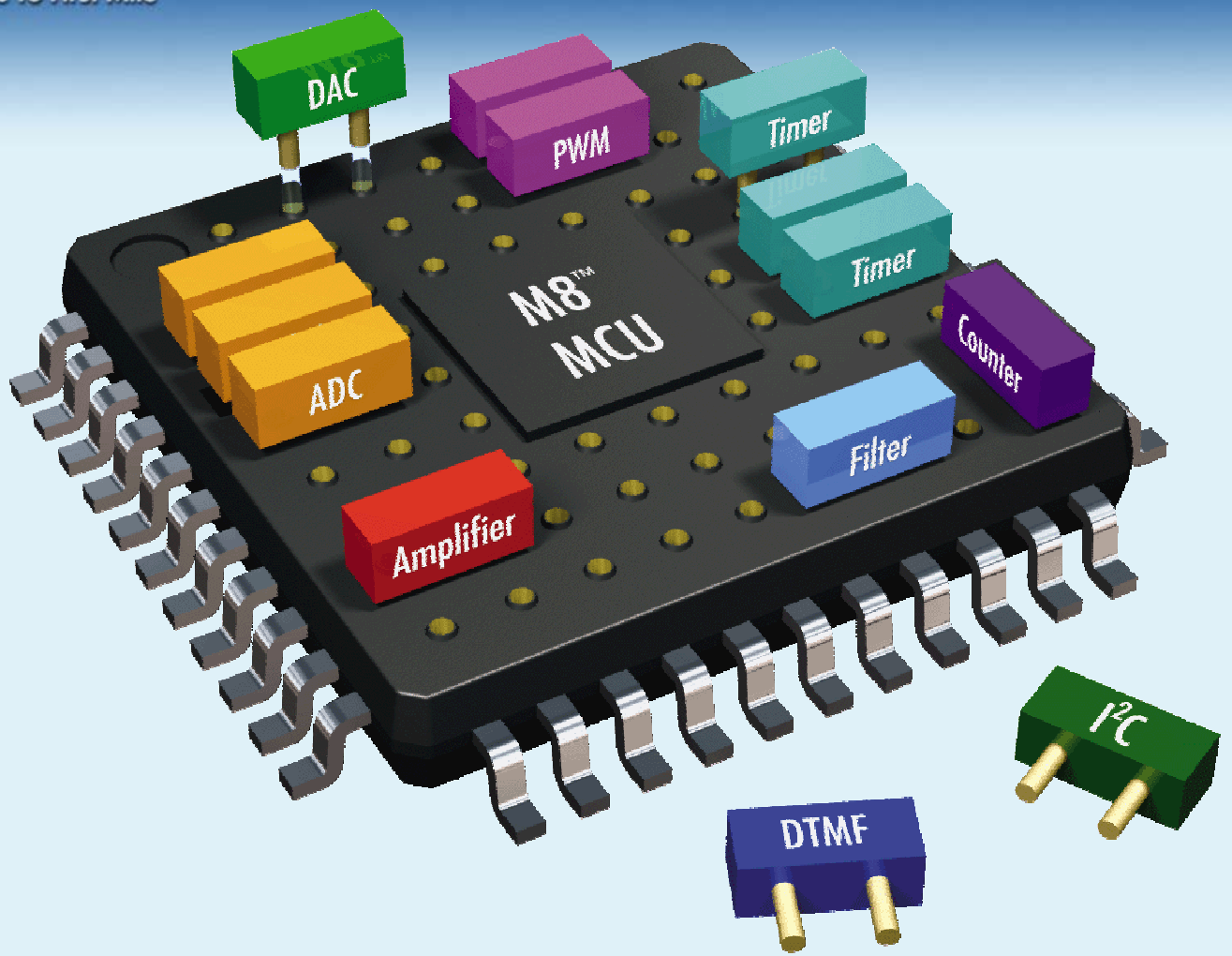
The next PSoC Teletraining class is Module 2. In this module you will develop a much more challenging MCU. The course will lead you through many more of the PSoC configurable features.

Module 3 is an advanced class using the PSoC Debugger.

Module 4 will then describe in detail the Registers, data sheets, Analog and Digital Blocks, and demonstrate dynamic reconfiguration.

Thank you. Please join us for the other Modules!

CYPRESS
Connecting From Last Mile to First Mile™



Thank you for making PSoC an overwhelming success !

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