SD Card Specification

Model Name :

KP032S3CBS

KP032S3CCS

KP064S3DAS

KP128S3EMS

KP256S3EMS

KP256S3FMS

KP512S3EMS

KP512S3FMS

KP01GS3FMS

Ver 1.1

07.08.200

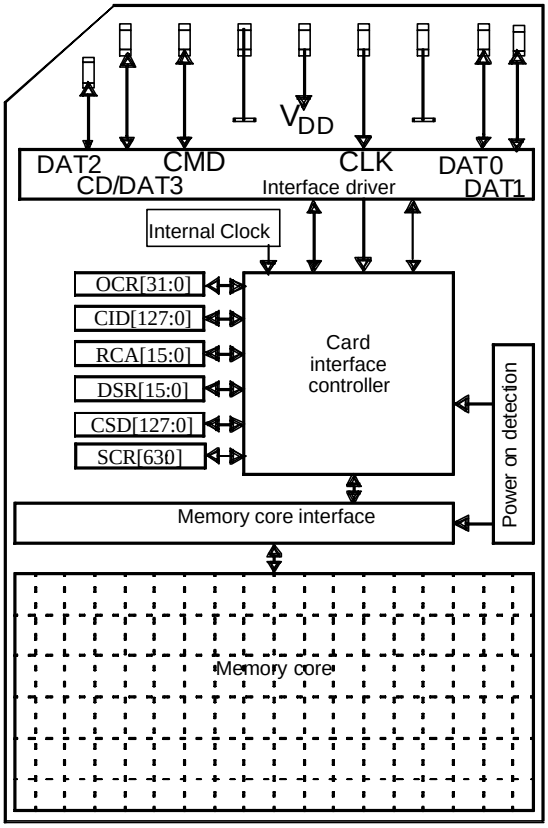
Features

- Capcity:32MB/64MB/128MB/256M/512MB/1GByte
- Compliant Specification Ver 1.01
- On card error correction
- Support CPRM
- Two alternative communication protocols:
  SD mode and SPI mode
- Variable clock rate 0~25MHz.
- Voltage range for communication: 2.0~3.6V
  for operating :2.7~3.6V.
- Low power consumption : automatic power down and automatic wake up, smart power management
- No external programming voltage required.
- Damage free powered card insertion and removal
- Forward compatibility to MultiMedia Card.
- High speed serial interface with random access
  ---support dual channels with interleave for flash memory.
  ---QuickWrute™ Technology: a cost-effective solution with ultra high performance of flash access time and high reliability of data storage.
  ---Max. Read/Write rate :10Mbyte/s
- Up to 10 stacked card(at 20MHZ,VCC=2.7~3.6V)
- Data Endurance: 100k Program/Erase Cycles
- CE and FCC certificates
- PIP package Technology
- Dimension: 24mm(W)x32mm(L)x1.4mm(T)

Description

These SD cards are highly integrated flash memories with serial and random access capability. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission. This interface allows several cards to be stacked by through connecting their peripheral contacts. These SD cards are fully compatible to a new consumer standard, called the SD Card system standard define in the SD card System specification. The SD card system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. SD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors mobile, battery-powered application such as audio players, organizers, palmtops, electronic books, encyclopedia and dictionaries. Using very effective data compression schemes such as MPEG, the SD card will deliver enough capacity for all kinds of multimedia data.

Block Diagram



All units these SD card are clocked by an internal clock generator. The interface driver unit synchronizes the DAT and CMD signals from external CLK to the internal used clock signal. The card is controlled by the six line SD card interface containing the signals: CMD,CLK,DAT0~DAT3. For the identification of the SD card in a stack of SD card, a card identification register(CID) and a relative and address register(RCA) is foreseen. An additional register contain different types of operation parameter. This register is called(CSD). The communication using the SD card lines to access either the memory field or the register is defined by the SD card standard. The card has its own power on detected unit. No additional master reset signal is required to setup the card after power on. It is protected against short circuit during insertion and removal while the SD card system is power up. No external programming Voltage supply is required. The programming voltage is generated on card. These SD card support a second interface operation mode the SPI interface mode. The SPI mode is active if the CS signal is asserted(negative) during the reception of the reset command(CMD0).

Interface

These SD Card interface can operate in two different modes:

. SD Card mode

. SPI mode

Host system can choose either one of modes. SD Card mode allow the 4-bit high performance data transfer. SPI mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss performance, relatively to the SD mode.

SD Card mode pin definition

Pin	Name	Type[1]	Description
1	CD DAT3	I/O/PP	Card Detect Data bit 3
2	CMD	PP	Command/Response
3	V_{SS1}	S	Ground
4	V_{CC}	S	Supply Voltage
5	CLK	I	Clock
6	V_{SS2}	S	Ground
7	DAT0	I/O/PP	Data bit 0
8	DAT1	I/O/PP	Data bit 1
9	DAT2	I/O/PP	Data bit 2

1: S: Power Supply, I: Input O: Output I/O: Bi-directionally PP: I/O using push-pull drivers

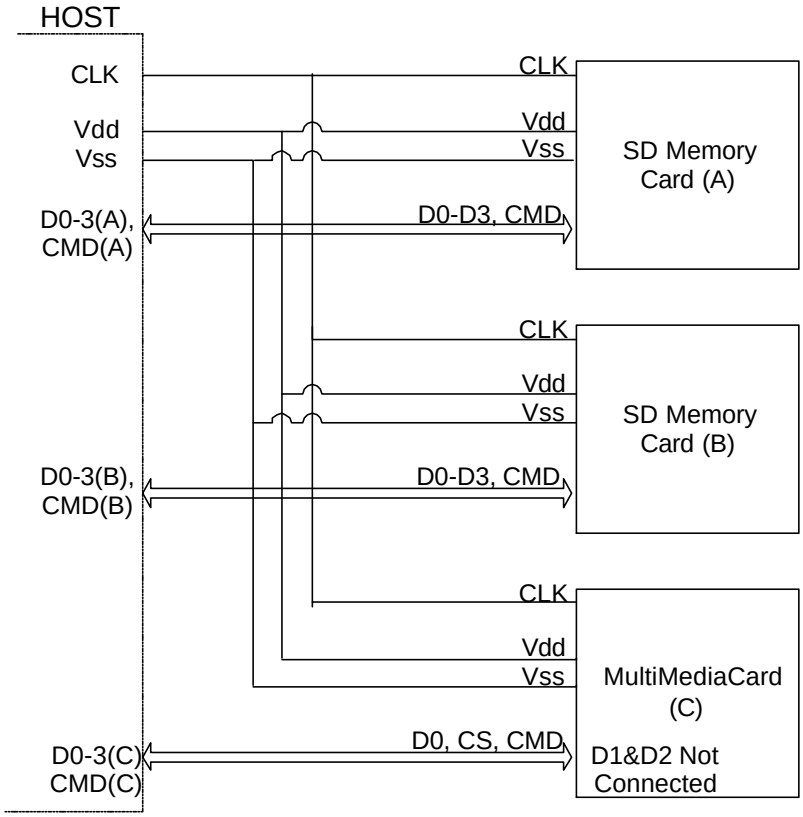
SD Card Bus Concept

The SD bus allows the dynamic configuration of the number of dsts line from 1 to 4 Bi-directional data signal.
After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width.
Multiplied SD cards connections are available to the host. Common $V_{CC,}$ $V_{ss,}$ and CLK signal connections are available in the multiple connection. However, Command, Respond and Data line(DAT0~DAT3) shall be divided for each card from host.
This feature allows easy trade off between harware cost and system performance. Communication over the SD bus Is based on command and data bit stream initiated by a start bit terminated by stop bit.

CLK: with each cycle of this signal a one bit transfer on the command and data lines are done. The frequency may vary between zero and the maximum clock frequency. The SD Card bus master is free to generate these cycles without restriction in the range of 0 to 25Mhz.

CMD: Commands are transfer serially on the CMD line. A command is a token to starts an operation from host to the card. Commands sent to a address single card(address command) or to all connected cards(boardcast command). Responses are transfer serially on the CMD line. A response is a token to answer to a previous command. Responses Are sent from a single card or from all connected cards.

DAT0~3: Data can be transfer from the card to host or vice versa. Data is transferred via the data line.



SD Card bus Topology

SPI mode pin definition

Pin	Name	Type[1]	Description
1	CS	I	Chip Select(Neg. True)
2	DI	I	Data In
3	V_{SS1}	S	Ground
4	V_{CC}	S	Supply Voltage
5	CLK	I	Clock
6	V_{SS2}	S	Ground
7	DO	O	Data Out
8	RSV	-	
9	RSV	-	

1 S: Power Supply, I: Input O: Output I/O: Bi-directionally PP: I/O using push-pull drivers

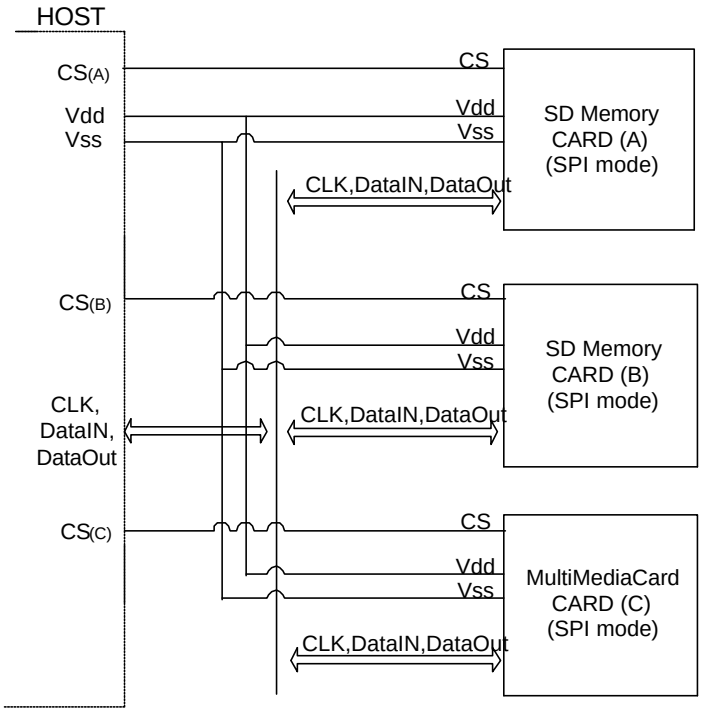
Note: These signals should be pulled up by host side with 10~100K ohm resistance in the SPI mode.

SPI Bus Concept

The SPI bus allows one bit data line by 2-chanel(Data In and Out). The SPI compatible mode allows the MMC Host systems to use SD card with little change. SPI mode is byte transfers.

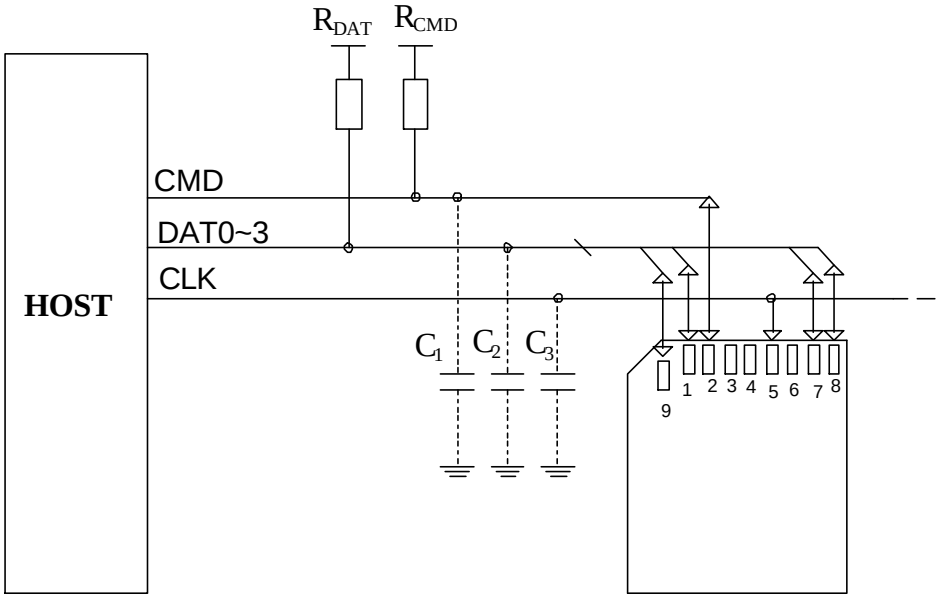
All the data token are multiples of the bytes(8 bit) and always byte aligned to the CS signal. The advantage of the SPI mode is reduceing the host design in effort. Especially, MMC host can be modified with little change.

The disadvantage of the SPI mode is the loss of performance versus SD card mode.



SPI mode bus topology

SD Card Electrical Characteristics



SD card Connection diagram

DC Characteristic

ABSOLUTE MAXIMUM RATINGS

The maximum rating is the limit value that must not be exceeded even at an instant. As long as you use the product within the maximum rating defined, no permanent damage will ever be occurred. However this does not guaranteed the normal logical operation.

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V_{CC}	-0.3	4.6	V	
ESD (contact Pads)		-4	4	KV	
Storage Temperature	T_{STG}	-40	85	℃	
Storage Humidity	40℃, 93%				

Bus Signal Li ne Load

Parameter	Symbol	Min.	Max.	Unit	Note
Pull-up resistance for CMD	R_{CMD}	10	100	KO	Prevent bus floating
Pull-up resistance for DAT	R_{DAT}	10	100	KO	Prevent bus floating
Bus Signal Line Capacitance	C_L	-	250	pF	F_{pp} <5MHz,21cards
Bus Signal Line Capacitance	C_L	-	1000	pF	F_{pp} <20MHz, 7cards
Signal Card Capacitance	C_{CARD}	-	10	pF	
Maximum Signal line Inductances		-	16	nH	F_{pp} <20MHz
Pull-up resistance inside card(Pin1)	R_{DAT3}	10	90	KO	May be used for card detecion

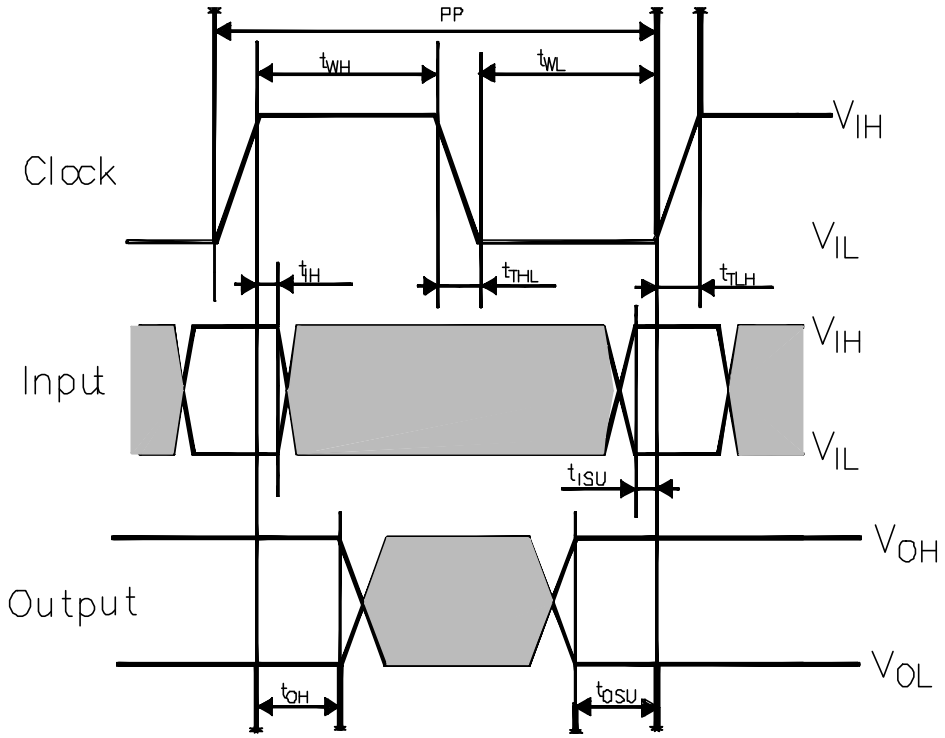
Operating Rating

Parameter	Symbol	Min.	Max.	Unit	Note
Operation Temperature	T_{OTG}	-25	85	℃	
Supply Voltage	V_{CC}	2.0	3.6	V	
Supply Voltage Specified in OCR Register		2.7	3.6	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.25x V_{CC}	V	
Input High Voltage	V_{IH}	0.625x V_{CC}	V_{CC}+0.3	V	
Output Low Voltage	V_{OL}		0.125x V_{CC}	V	I_{OL}=100uA@VDD Min
Output High Voltage	V_{OH}	0.75x V_{CC}		V	I_{OH}= -100uA@VDD Min
Input Leakage Current		-10	10	uA	
Output Leakage Current		-10	10	uA	
Standby current			150	uA	At 0Hz, 3.6V Standby state
High Speed Supply current			80	mA	At 25Hz, 3.6V
Operation Humidity	25℃, 95%				

AC Characteristic

Bus Timing

Parameter	Symbol	Min.	Max.	Unit	Note
Clock Frequency Data Transfer Mode	F_{PP}	0	25	MHz	C_L≤100pF(7Cards)
Clock Frequency identification Mode	F_{OD}	0	400	KHz	C_L≤250pF(21Cards)
Clock Low time	t_{WL}	10		ns	C_L≤100pF(7Cards)
Clock High time	t_{WH}	10		ns	C_L≤100pF(7Cards)
Clock Rise time	T_{TLH}		10	ns	C_L≤100pF(7Cards)
Clock Fall time	T_{THL}		10	ns	C_L≤100pF(7Cards)
Clock Low time	t_{WL}	50		ns	C_L≤250pF(21Cards)
Clock High time	t_{WH}	50		ns	C_L≤250pF(21Cards)
Clock Rise time	T_{TLH}		50	ns	C_L≤250pF(21Cards)
Clock Fall time	T_{THL}		50	ns	C_L≤250pF(21Cards)
Input Set-up Time	T_{ISU}	5		ns	CMD,DAT Reference to CLK
Input Hold Time	T_{IH}	5		ns	CMD,DAT Reference to CLK
Output Set-up Time	T_{OSU}	5		ns	CMD,DAT Reference to CLK
Output Set-up Time	T_{OH}	5		ns	CMD,DAT Reference to CLK



Transfer Rate

Testing Condition

1. Main Board: Abit BG7

2. CPU: Intel Pentium 4 2GHz

3. DDR Memory: 256MByte

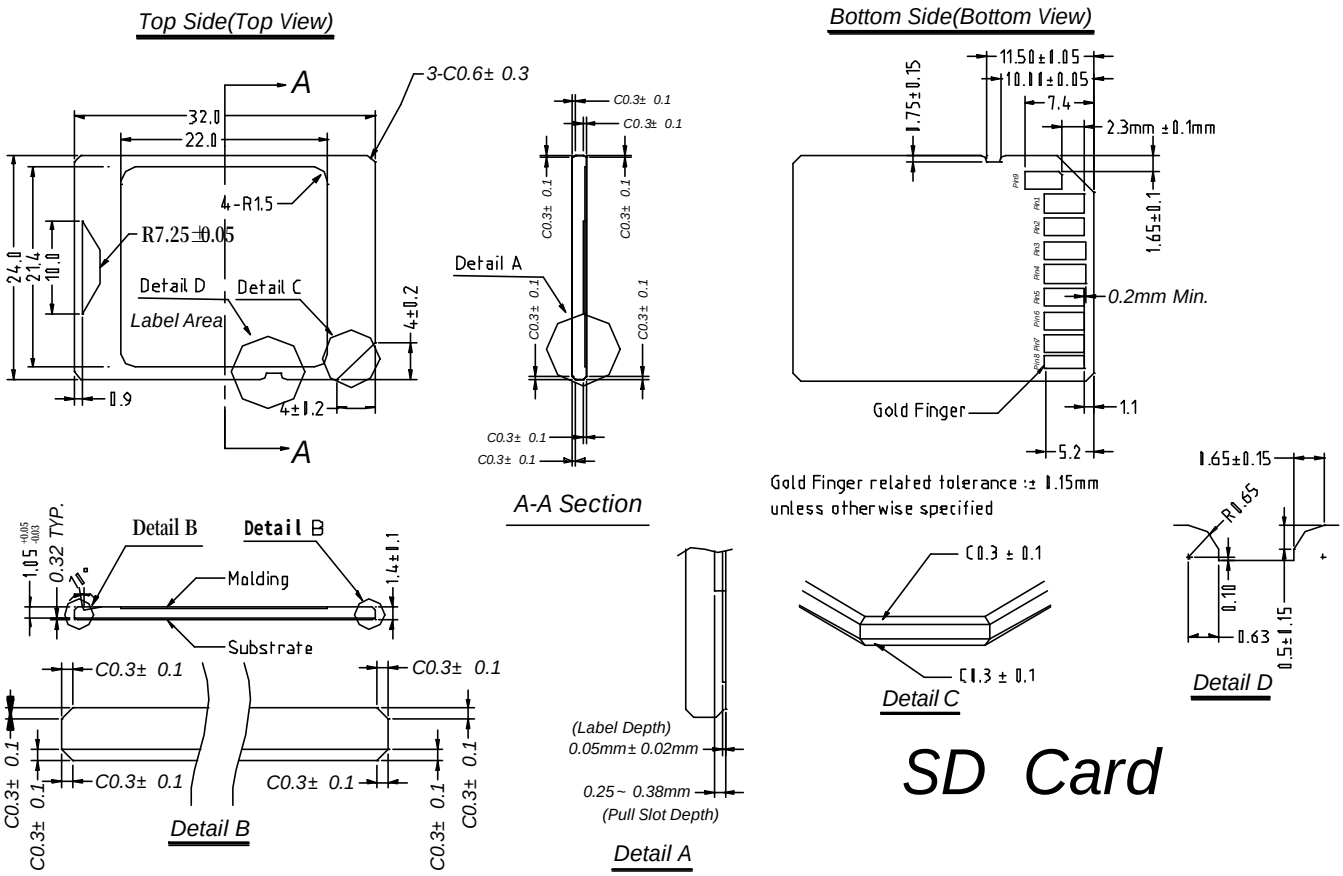
4. OS: XP with SP1

5. Software: HD Bench Ver3.4

6. Testing Device: SD card with USB 2.0 Card Reader(SM320T)

Capacity	Sequential Read	Sequential Write	Random Read	Random Write	Unit
32MB	6236	1562	6360	710	KB/s
64MB	6617	3386	6551	1269	KB/s
128MB	6858	6009	6824	1538	KB/s
256MB	8912	7843	8854	1592	KB/s
512MB	9225	8139	9098	1506	KB/s
1GB	9229	8238	9098	1848	KB/s

Physical Outline Dimension



All dimension tolerances are ± 0.1mm, unless otherwise specified.