Nové bloky v moderných obvodoch FPGA

Obsah

- hierarchické pamäťové subsystémy,
- obvody PLL a DLL pre syntézu a distribúciu hodinových signálov,
- vložené (embedded) procesorové jadrá,
- hardvérové násobičky, DSP bloky,
- štruktúra logických blokov (LE, CLB),
- podpora nových IO štandardov,
- podpora pre dešifrovanie konfiguračných dát, on-line dekompresia.

Preberaná problematika bude demonštrovaná na vybraných **najnovších** produktoch firiem Altera, Xilinx a Actel. Analyzované vylepšenia a princípy sú však používané aj inými výrobcami obvodov FPGA.

Prehľad najnovších obvodov FPGA

Altera Stratix II

General-purpose FPGA family with the largest density & fastest performance

- Nios II embedded processor support
- The most DSP blocks
- Large on-chip memory
- High-speed I/O & memory interfaces
- 1-Gbps dynamic phase alignment (DPA) with source-synchronous signaling
- Broad IP portfolio support

Table 1–1. Stratix II FPGA Family Features

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) *(1)*	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs *(2)*	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
M4K RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers *(3)*	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

Notes to Table 1–1:

(1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus II software for logic synthesis.
(2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).
(3) These multipliers are implemented using the DSP blocks.

Altera Cyclone II
Second-generation, lowest-cost family in the Cyclone™ FPGA series for designs where cost concerns outweigh the need for performance or extensive features

- Nios® II embedded processor support
- Embedded 18x18 digital signal processing (DSP) multipliers
- Moderate on-chip memory
- Moderate-speed I/O & memory interfaces
- Broad intellectual property (IP) portfolio support

Table 1–1. Cyclone II FPGA Family Features

Feature	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	105	129	250
Total RAM bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded multipliers *(1)*	13	18	26	35	86	150
PLLs	2	2	4	4	4	4
Maximum user I/O pins	142	182	315	475	450	622

Note to Table 1–1:
(1) This is the total number of 18 × 18 multipliers. For the total number of 9 × 9 multipliers per device, multiply the total number of 18 × 18 multipliers by 2.

Altera Hardcopy II
Low-cost structured ASIC solution with:

- Fine-grained structured cell architecture
- Prototype with Stratix II FPGA
- Same design flow as Stratix II FPGA

- All Stratix II features
- Guaranteed seamless migration of FPGA-proven designs
- Supported by all major EDA vendors
- 50 percent lower power than Stratix II FPGA
- 350-MHz performance
- Broad IP portfolio support

Xilinx Virtex 4

- 200,448 logic cells, 30 percent more logic resources than the closest competitor
- 15 percent faster fabric on average than the closest competing 90nm FPGA

- 6,048 Kbits of 500 MHz block RAM with unique built-in FIFO control logic and ECC for highest performance and lowest power consumption
- 96 XtremeDSP™ slices, each supporting 500 MHz 18x18 multiply and accumulate (MAC) operations while consuming a mere 2.3 mW/100 MHz
- Up to 960 I/Os (448 differential pairs) with unique ChipSync™ source-synchronous circuitry in every I/O
- Hardware-proven support for all major memory interfaces including DDR2 SDRAM, DDR SDRAM, QDR II SRAM, and RLDRAM II
- As much as 5 Watts lower power per FPGA compared to competing 90nm FPGAs as a result of unique triple-oxide technology and embedded IP

Table 1: **Virtex-4 FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)(1)				XtremeDSP Slices(2)	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transciever Blocks	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VLX15	64 x 24	13,824	6,144	96	32	48	864	4	0	N/A	N/A	N/A	9	320
XC4VLX25	96 x 28	24,192	10,752	168	48	72	1,296	8	4	N/A	N/A	N/A	11	448
XC4VLX40	128 x 36	41,472	18,432	288	64	96	1,728	8	4	N/A	N/A	N/A	13	640
XC4VLX60	128 x 52	59,904	26,624	416	64	160	2,880	8	4	N/A	N/A	N/A	13	640
XC4VLX80	160 x 56	80,640	35,840	560	80	200	3,600	12	8	N/A	N/A	N/A	15	768
XC4VLX100	192 x 64	110,592	49,152	768	96	240	4,320	12	8	N/A	N/A	N/A	17	960
XC4VLX160	192 x 88	152,064	67,584	1056	96	288	5,184	12	8	N/A	N/A	N/A	17	960
XC4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	N/A	N/A	N/A	17	960

Xilinx Spartan 3

The Spartan-3E FPGA family offers the optimal combination of platform features and low cost you need for high-volume, gate-centric programmable logic designs:

- Lowest Device Cost
  - 100K system gates for under US$2.00*
  - 1.2 million system gates for under US$9.00*
- Lowest Configuration Memory Device Cost
  - Added support for commodity serial (SPI) and parallel flash memory
  - Continuing support for low-cost Xilinx Platform Flash

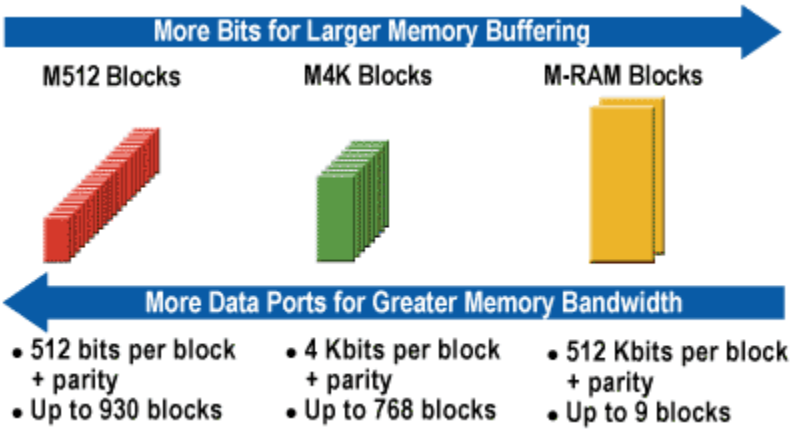
Spartan-3E FPGAs further reduce cost by integrating the functions of many discrete chips into a single FPGA, providing the lowest system cost:

- Lowest Embedded Processing Cost - Complete 32-bit MicroBlaze processor (68 D-MIPS) for an effective cost of $0.48*
- Lowest DSP Cost - 9.1 GMAC/s in XC3S1200E for an effective cost of less than $1.00/GMAC/s*

Hierarchické pamäťové subsystémy

Kombinácia vložených pamäťových blokov s rôznymi veľkosťami (a tiež cieľovým využitím):

TriMatrix štruktúra vložených pamätí v obvodoch Altera Stratix II



Typické využitie jednotlivých blokov

M512 Blocks	M4K Blocks	M-RAM Blocks
Rake receiver correlator	ATM cell packet processing	IP packet buffering
Shift register	Header/cell storage	System cache
Small FIFO buffers	Channelized functions	Video frame buffers
Finite impulse response (FIR) filter delay line	Program memory for processors	Echo canceller data storage
		Processor code storage

Veľkosti pamätí v dostupných obvodoch Stratix II

Table 1. Memory Resources in Stratix Devices

Device	M512 Blocks	M4K Blocks	M-RAM Blocks	Total Memory Bits
EP2S15	104	78	0	419,328
EP2S30	202	144	1	1,369,728
EP2S60	329	255	2	2,544,192
EP2S90	488	408	4	4,520,448
EP2S130	699	609	6	6,747,840
EP2S180	930	768	9	9,383,040

Základné vlastnosti

Table 2. TriMatrix Memory Features

Memory Feature	M512 Blocks 512-bits + Parity	M4K Blocks 4-Kbits + Parity	M-RAM Blocks 512-Kbits + Parity
Maximum Performance	380 MHz	400 MHz	400 MHz
True Dual-Port Memory	No	Yes	Yes
Simple Dual-Port Memory	Yes	Yes	Yes
Single-Port Memory	Yes	Yes	Yes
Address Enable	No	Yes	Yes
Byte Enable	No	Yes	Yes
Parity Bits	Yes	Yes	Yes
Shift Register	Yes	Yes	Yes
Mixed-Clock Mode	Yes	Yes	Yes
Memory Preload	Yes	Yes	No
Configurations	512 x 1 256 x 2 128 x 4 64 x 8 64 x 9 32 x 16 32 x 18	4K x 1 2K x 2 1K x 4 512 x 8 512 x 9 256 x 16 256 x 18 128 x 32 128 x 36	64K x 8 64K x 9 32K x 16 32K x 18 16K x 32 16K x 36 8K x 64 8K x 72 4K x 128 4K x 144

Obvody PLL a DLL pre syntézu a distribúciu hodinových signálov

Cieľ:

Clock Deskew – eliminácia oneskorenia pri šírení hodinových signálov v rámci FPGA čipu

Frequency Synthesis – vytváranie hodinových signálov ktoré sú násobkom (aj neceločíselným) vstupného hodinového signálu. Základné výhody on-chip syntézy:

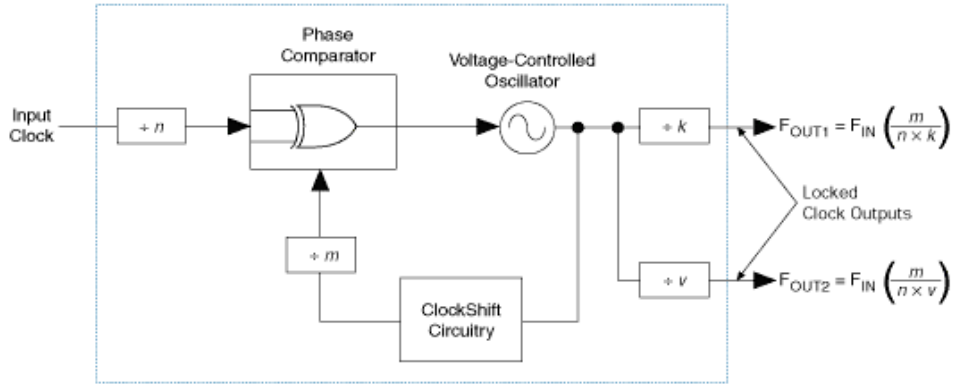
- väčšia flexibilita návrhu
- menšie rušenie

Phase Shifting – vytváranie signálov s nastaviteľnými fázovými posunmi

Rôzne princípy:

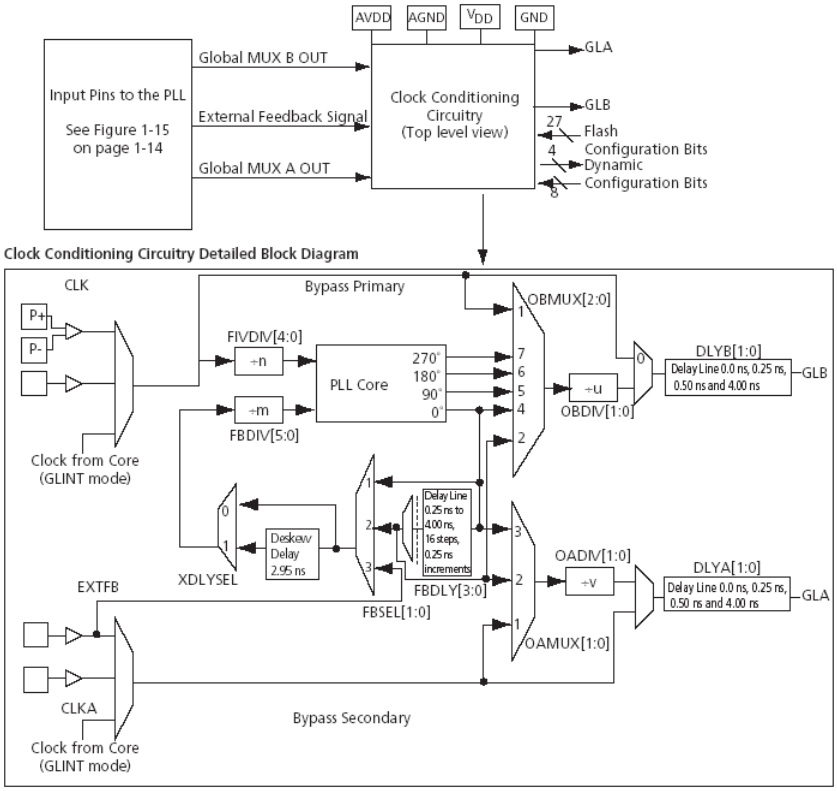
Altera PLL (**Phase Locked Loop**) – využitie analógových závesov

Princíp PLL



- zvyšujú sa rozsahy násobiacich a deliacich faktorov
- rozsahy vstupných a výstupných frekvencii
- frekvencii VCO
- počty PLL na čipe a počty výstupov jednotlivých PLL sa zvyšujú

PLL v obvodoch Actel ProASIC



Notes:

1. *FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.*
2. *DLYA, DLYB, DLYAFB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.*
3. *OBDIV will also divide the phase-shift since it takes place after the PLL Core.*

Figure 1-14 • **PLL Block – Top-Level View and Detailed PLL Block Diagram**

Stratix II obvody PLL

- Up to 16 global clocks with 24 clocking resources per device region
- Clock control block supports dynamic clock network enable/disable, which allows clock networks to power down to reduce power consumption in user mode
- Up to 12 PLLs (four **enhanced** PLLs and eight **fast** PLLs) per device provide **spread spectrum**, programmable bandwidth, clock switchover, real-time PLL reconfiguration, and advanced multiplication and phase shifting

Xilinx DLL (**Digital Ľocked Loop**) – využitie knfigurovateľných oneskorovacích liniek

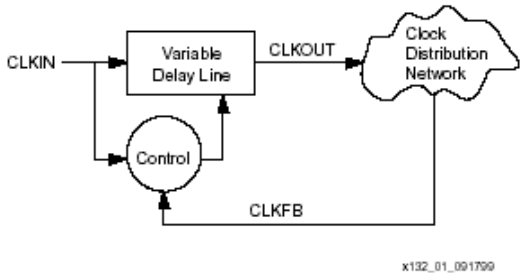


Figure 1: **Delay-Locked Loop Block Diagram**

As shown in Figure 1, a DLL in its simplest form consists of a variable delay line and control logic. The delay line produces a delayed version of the input clock CLKIN. The clock distribution network routes the clock to all internal registers and to the clock feedback CLKFB pin. The control logic must sample the input clock as well as the feedback clock in order to adjust the delay line.

Delay lines can be built using a voltage controlled delay or a series of discrete delay elements. For optimum performance the Xilinx DLL uses a discrete digital delay line.

A DLL works by inserting delay between the input clock and the feedback clock until the two rising edges align, putting the two clocks 360 degrees out of phase (meaning they are in phase). After the edges from the input clock line up with the edges from the feedback clock, the DLL "locks." As long as the circuit is not evaluated until after the DLL locks, the two clocks have no discernible difference. Thus, the DLL output clock compensates for the delay in the clock distribution network, effectively removing the delay between the source clock and its loads.

Príklad využitia DLL na vytvorenie signálov pre DDR (Double Data Rate) pamäte

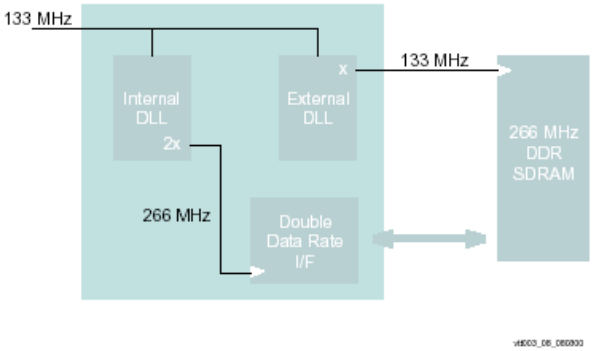


Figure 8: **Virtex-E FPGA Interfacing With a 266 MHz DDR SDRAM Memory Module**

Využitie PLL na kopenzáciu oneskorenia hodinového signálu (Actel)

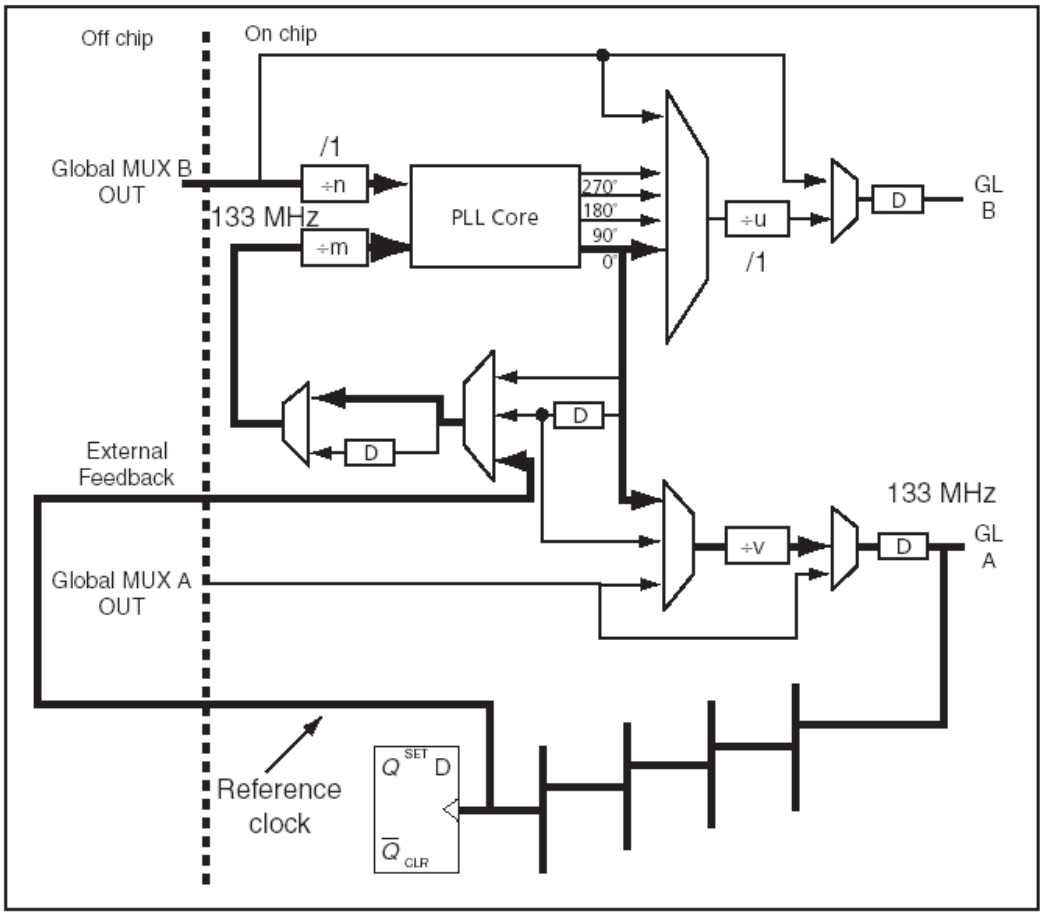
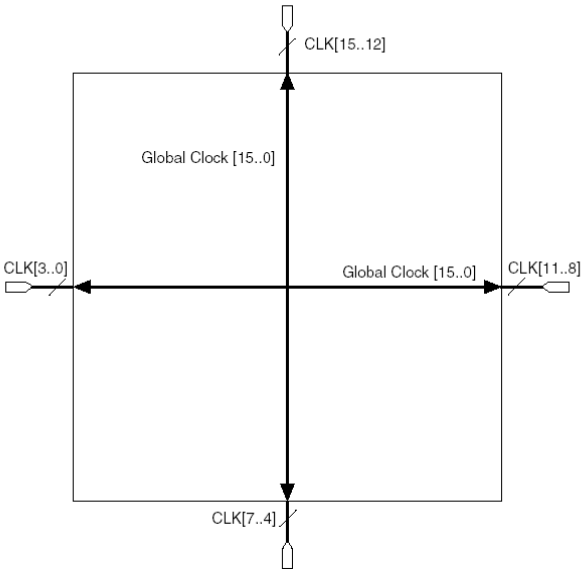


Figure 1-20 • **Using the PLL for Clock Deskewing**

Distribúcia hodinových signálov do všetkých častí obvodu (s minimálnym oneskorením) vyžaduje rozsiahlu prepojovaciu sieť:

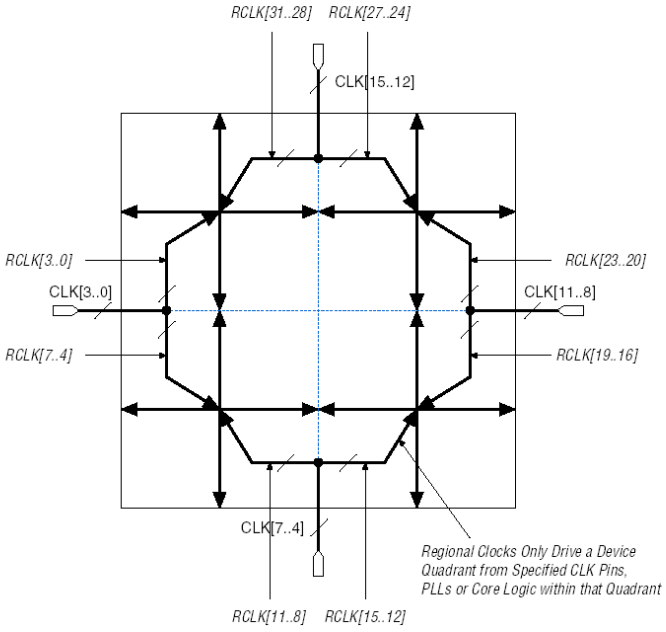
Global clock network v obvodoch Stratix II

Figure 2–31. Global Clocking



Regional clock network v obvodoch Stratix II

Figure 2–32. Regional Clocks



Vložené (embedded) procesorové jadrá

Kapacita moderných obvodov FPGA umožňuje začlenenie procesorových jadier do obvodov FPGA:

Hard cores – procesor je na spoločnom čipe s FPGA obvodom, je však vytvorený počas výroby FPGA obvodu

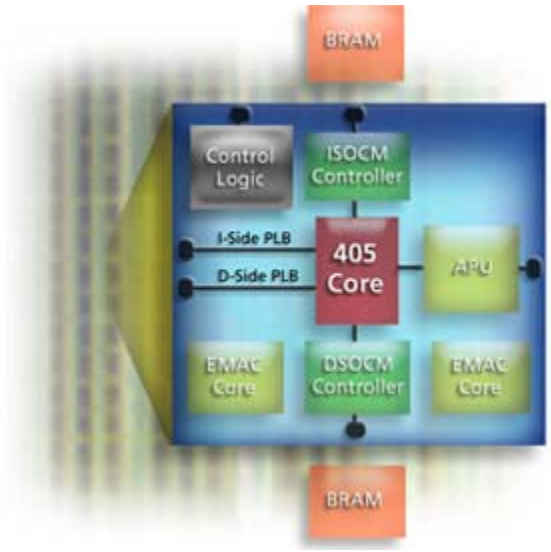
- Altera Excalibur (200 MHz ARM922T processor + FPGA)
- Xilinx PowerPC

Soft cores – processor(y) je využívajú zdroje FPGA (vložené pamäte, logické elementy)

- Altera Nios II
- Xilinx 8-bit PicoBlaze, 32-bit MicroBlaze

Xilinx PowerPC™ RISC Processor

The Virtex-4™ FX platform FPGAs provides up to two PowerPC™ 405, 32-bit RISC processor cores in a single device. These industry standard processors offer high performance and a broad range of third-party support. The new Auxiliary Processor Unit (APU) controller simplifies the integration of hardware accelerators and co-processors.



PowerPC Features:

- Embedded PowerPC 405 (PPC405) core
  - Embedded 450 MHz, 700+ DMIPS RISC core (32-bit Harvard architecture)
  - 5-stage data path pipeline
  - Hardware multiply and divide
  - 32 x 32-bit general-purpose registers
  - 16 KB 2-way set-associative instruction and data caches
  - Memory Management Unit (MMU) enables RTOS implementation
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1KB - 16 KB)
  - Enhanced instruction and data On-Chip Memory (OCM) controllers interface directly to embedded Block RAM

    - Supports IBM CoreConnect™ bus architecture
    - Debug and trace support
- New Auxiliary Processor Unit (APU) controller interfaces the CPU pipeline directly to the FPGA fabric.
    - Enables Hardware Accelerators
    - Supports User Defined Instructions
    - Supports up to four 32bit word data transfers in a single instruction
    - Floating point and co-processor support
    - Supports autonomous instructions: no pipeline stalls
    - 32-bit instruction and 64-bit data
    - 4-cycle cache line transfer
- Provides direct interface to Tri-mode Ethernet MAC configuration registers

Table 1. Altera Excalibur Devices

Feature	EPXA1	EPXA4	EPXA10
APEX Device-like Architecture	EP20K100E	EP20K400E	EP20K1000K
Maximum System Gates	263,000	1,052,000	1,772,000
Typical Gates	100,000	400,000	1,000,000
Logic Elements	4,160	16,640	38,400
Embedded System Blocks (ESBs)	26	104	160
Maximum RAM Bits	53,248	212,992	327,680
Maximum Macrocells	416	1,664	2,560
Maximum User I/O Pins	178	360	521
Single-Port SRAM (Kbytes)	32	128	256
Dual-Port SRAM (Kbytes)	1x16	2x32	2x64
Embedded Trace Module	-	ETM9	ETM9
Package (mm)	**Maximum User I/O Pins**		
484-Pin FineLine BGA$^{Â®}$ Package *(1)* 23x23	173	-	-
672-Pin FineLine BGA Package *(2)* 27x27	178	275	-
1,020-Pin FineLine BGA Package *(3)* 33x33	-	360	521

Xilinx PicoBlaze - veľmi malý 8-bitový procesor

PicoBlaze is a fully embedded 8-bit microcontroller macro for the Virtex™ and Spartan™ series of FPGAs and CoolRunner™-II CPLDs. The PicoBlaze reference designs support 57 to 59 different 16- or 18-bit instructions, 8 to 32 general-purpose byte-wide registers, up to 256 directly and indirectly addressable ports, reset, and a maskable interrupt. The PicoBlaze controller for Spartan-3, Virtex-4, Virtex-II, and Virtex-II Pro also include 64 bytes of scratchpad RAM.

Použiteľný tiež pre **CoolRunner-II and CoolRunner-IIA 1.8 Volt CPLD!!!**

Table 1: **CoolRunner-II CPLD Family Parameters**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Macrocells	32	64	128	256	384	512
Max I/O	33	64	100	184	240	270
T_{PD} (ns)	3.8	4.6	5.7	5.7	7.1	7.1
T_{SU} (ns)	1.9	2.0	2.4	2.4	2.9	2.6
T_{CO} (ns)	3.7	3.9	4.2	4.5	5.8	5.8
$F_{SYSTEM1}$ (MHz)	323	263	270	256	217	179

- Byte-wide Arithmetic Logic Unit (ALU) with CARRY and ZERO indicator flags
- 64-byte internal scratchpad RAM
- 256 input and 256 output ports for easy expansion and enhancement
- Automatic 31-location CALL/RETURN stack
- Predictable performance, always two clock cycles per instruction, up to 200 MHz or 100 MIPS in a Virtex-II Pro FPGA
- Fast interrupt response; worst-case 5 clock cycles
- Optimized for Xilinx Spartan-3, Virtex-II, and Virtex-II Pro FPGA architectures—just 96 slices and 0.5 to 1 block RAM
- Assembler, instruction-set simulator support

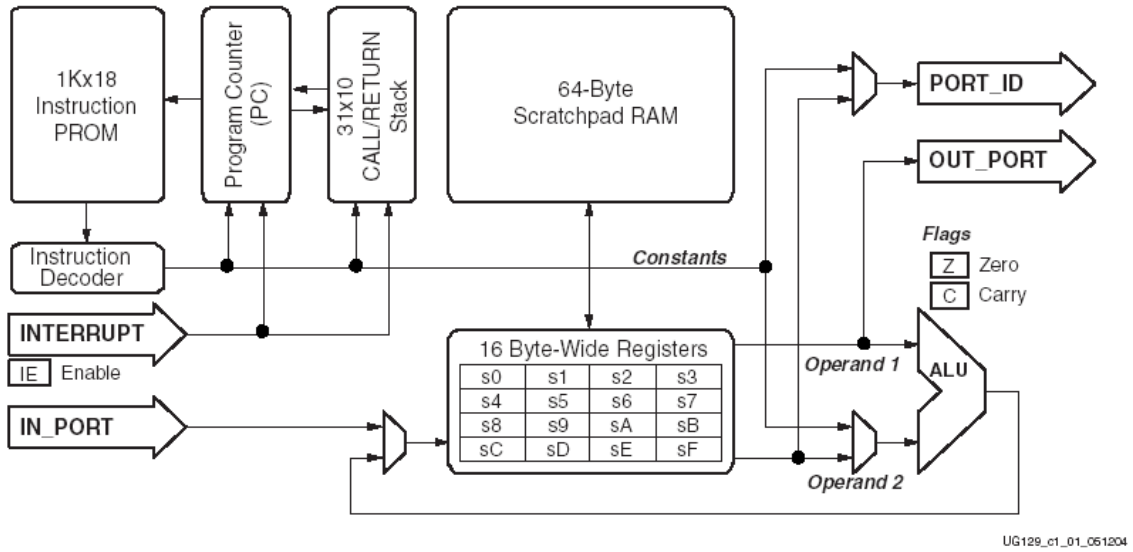


Figure 1-1: **PicoBlaze Embedded Microcontroller Block Diagram**

Summary of Nios II Processor Cores

Table 1. Altera Nios II Processor Core Summary

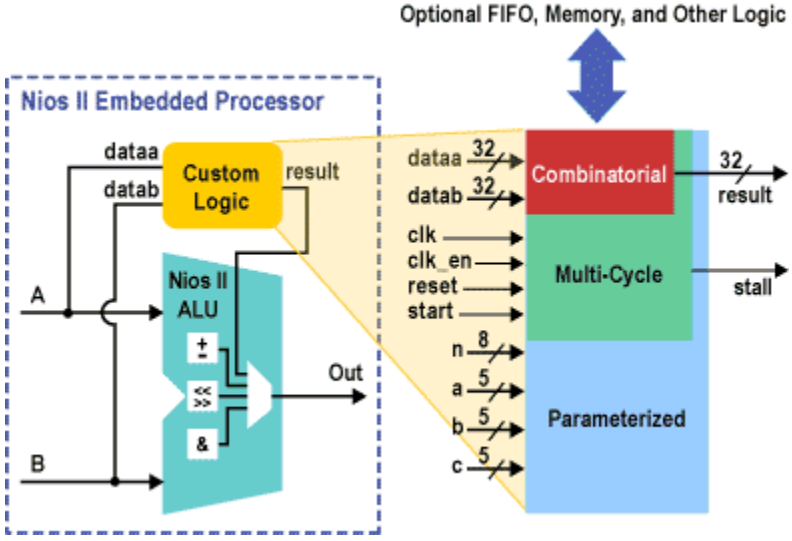
Features		Processor Cores		
		Nios II/e	Nios II/s	Nios II/f
Performance	DMIPS/MHz	0.16	0.75 (1)	1.17 (1)
	Max DMIPS	28	120 (1)	200 (1)
	f_{MAX}	Up to 150 MHz	Up to 135 MHz	Up to 135 MHz
Approximate size (in LEs)		<600	<1,300	<1,800
Pipeline stages		-	5	6
External address space		2 Gbytes	2 Gbytes	2 Gbytes
Instruction bus	Cache	-	512 bytes to 64 Kbytes	512 bytes to 64 Kbytes
	Branch prediction	-	Static	Dynamic
Data bus	Cache	-	-	512 bytes to 64 Kbytes
Arithmetic logic unit	Hardware multiply	-	3-Cycle (2)	1-Cycle (2)
	Hardware divide	-	-	Optional2
	Shifter	1 cycle-per-bit	3-cycle barrel shifter (2)	1-cycle barrel shifter (2)
JTAG debug module	JTAG interface, run-control, software breakpoints supported	Yes	Yes	Yes
	Hardware breakpoints supported	No	Yes	Yes
	Off-chip trace buffer supported	No	Yes	Yes
Exception handling	Integrated interrupt controller	Yes	Yes	Yes
Custom instruction support		256	256	256

Notes to Table 1:

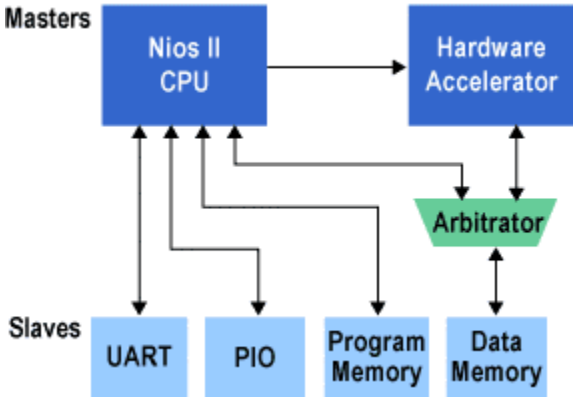
1. The Nios II/s and Nios II/f cores achieve higher DMIPS performance when targeting Altera devices with DSP blocks, such as Stratix II devices.
2. When targeting Altera devices without DSP blocks, the multiply, divide, and barrel shifter hardware is not available. In such cases, multiply and divide operations are emulated in software, and shift operations require one cycle per bit.

Typické výhody Soft procesorov:

Zákaznícke inštrukcie



Zákaznícke hardvérové akcelerátory (napr. pre šifrovanie, spracovanie signálov, ...)



Vývojové prostriedky (Altera)

- SOPC builder (integrovaný do Quartus II)
- Quartus II
- Embedded software design & debug tools (GNU C, debugger, …)
- Third paty tools (Modelsim, …)

Hardvérové násobičky, DSP bloky

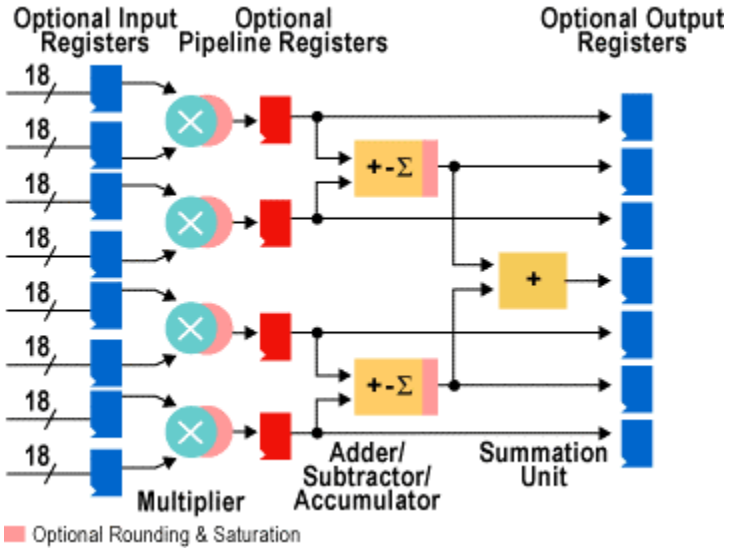
Ideálne pre aplikácie z oblasti:

- Image processing
- Wireless
- Military
- Broadcast
- Medical

Table 1. DSP Applications that Can Be Implemented Using DSP Blocks

Applications	Military Applications	Image Processing	Communications
	Radar	Broadcast & Medical	Wireless
Algorithms & Functions	• Filtering • Transforms • Modulation	• Filtering • Compression • Resizing	• Chip-Rate Processing • Equalization • Digital IF • Signal Data Rate (SDR)
Standards & Protocols	-	• JPEG 2000 • MPEG-4	• HSDPA • CDMA 2000, 1x EV DV

DSP Block Architecture (MAC operation support)



Detailná štruktúra DSP bloku pre konfiguráciu 18x18

Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration

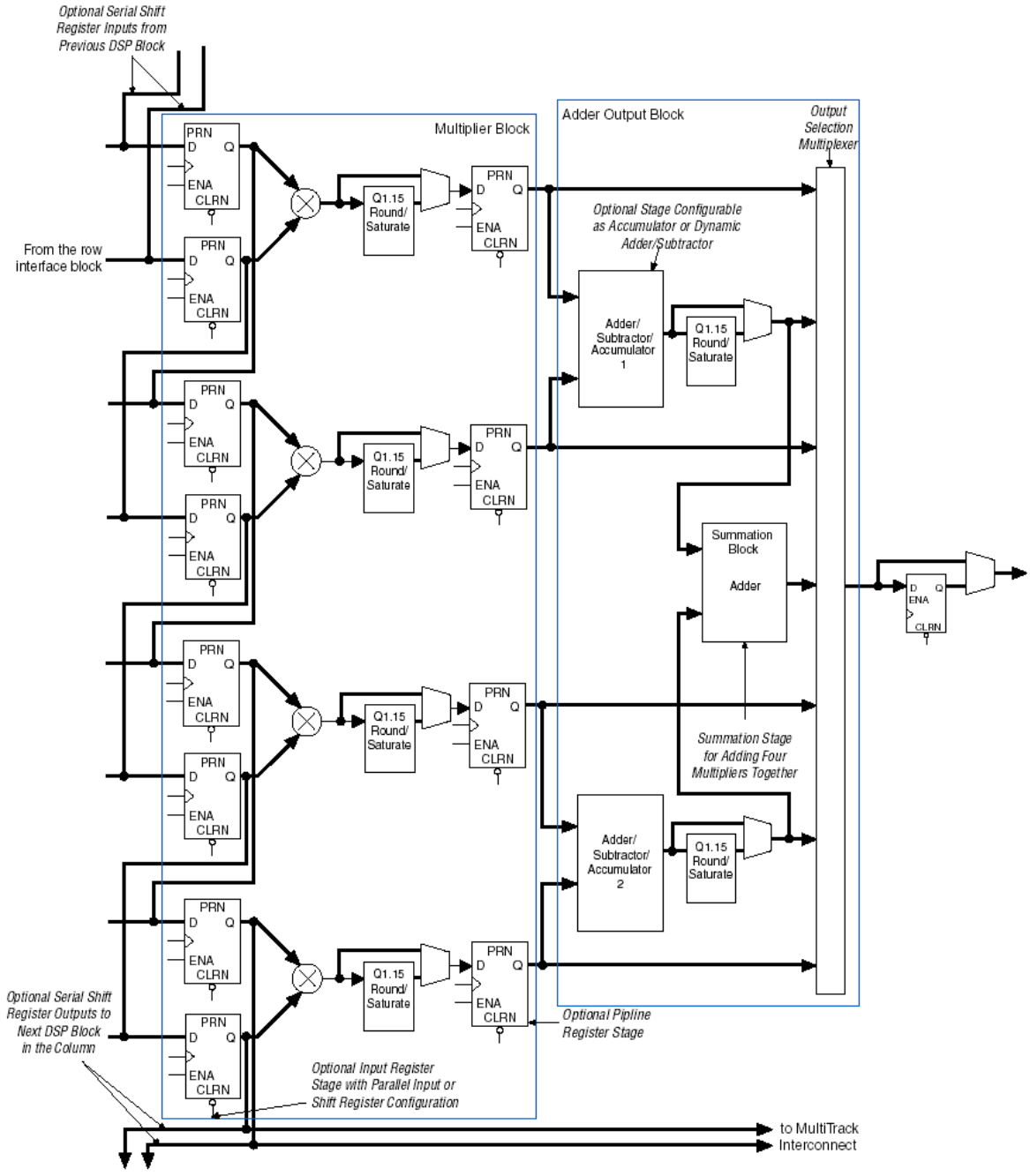


Table 6–1. Number of DSP Blocks in Stratix II Devices Note (1)				
Device	DSP Blocks	9 × 9 Multipliers	18 × 18 Multipliers	36 × 36 Multipliers
EP2S15	12	96	48	12
EP2S30	16	128	64	16
EP2S60	36	288	144	36
EP2S90	48	384	192	48
EP2S130	63	504	252	63
EP2S180	96	768	384	96

Note to Table 6–1:

(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

Figure 2–27. DSP Blocks Arranged in Columns

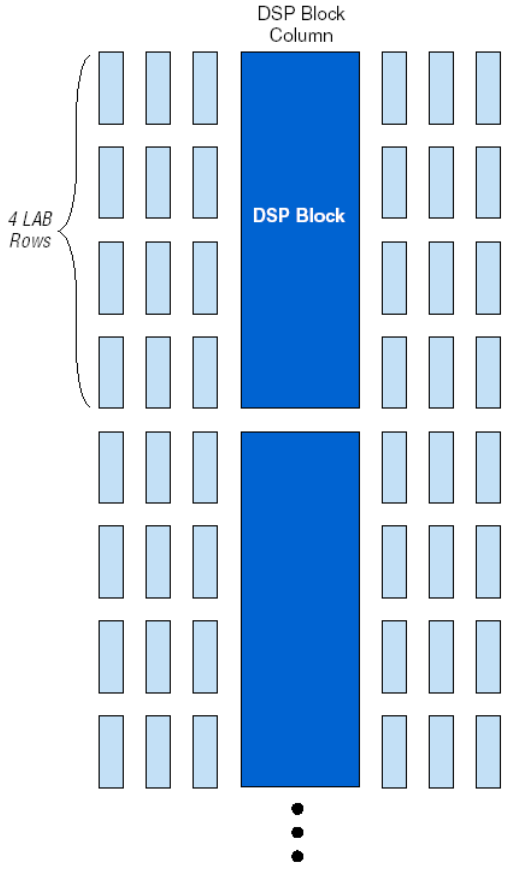


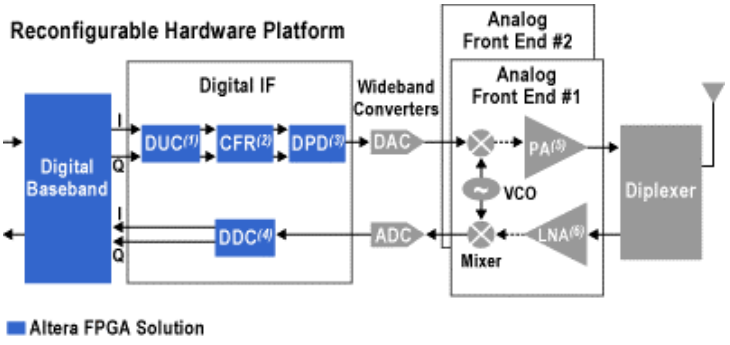
Table 6–5. DSP Block Operational Modes

Mode	Number of Multipliers		
	9 × 9	18 × 18	36 × 36
Simple multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier
Multiply accumulate	-	Two 52-bit multiply-accumulate blocks	-
Two-multiplier adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multiplier adder	Two four-multiplier adder	One four-multiplier adder	-

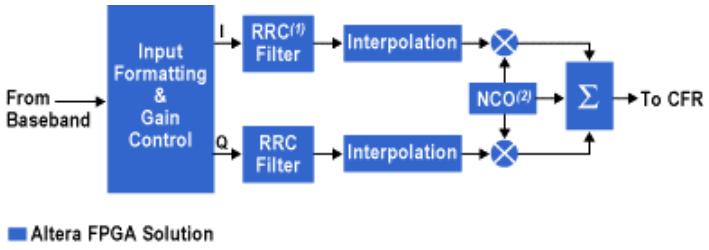
High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters

Príklady využitia DSP blokov v Softvérovo Definovanom Rádiu (SDR)

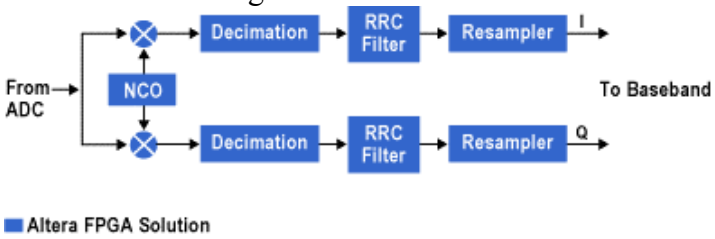
SDR architektúra založená na súčasnej FPGA technológii



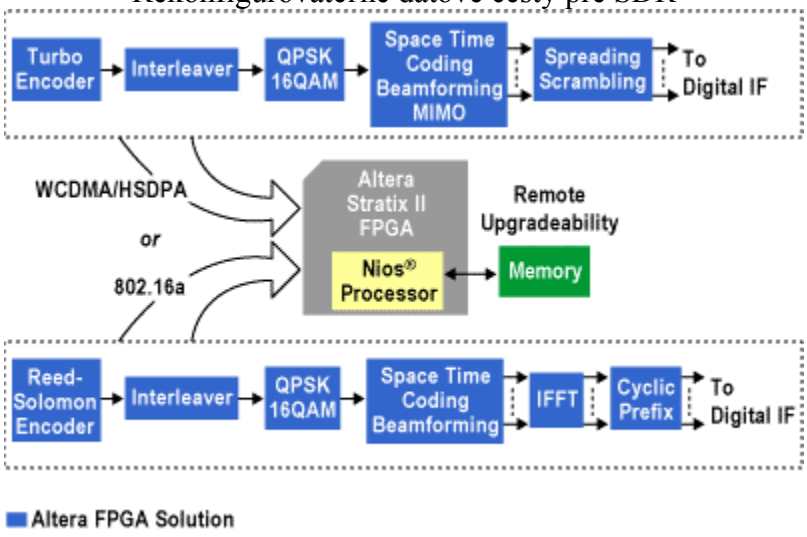
Digital downconverter



Digital downcorverter



Rekonfigurovateľné dátové cesty pre SDR



Štruktúra logických blokov (ALM, CLB)

Oproti starším rodinám FPGA obvodov obsahujú zložitejšie štruktúry logických blokov

Xilinx Virtex 4

CLB is optimized for area and speed for compact high performance design

4 slices per CLB implement any combinatorial and sequential circuit.

Each slice has 4-input look-up tables (LUT), flip-flops, multiplexors, arithmetic logic, carry logic, and dedicated internal routing.

Dedicated AND/OR logic implements wide input functions.

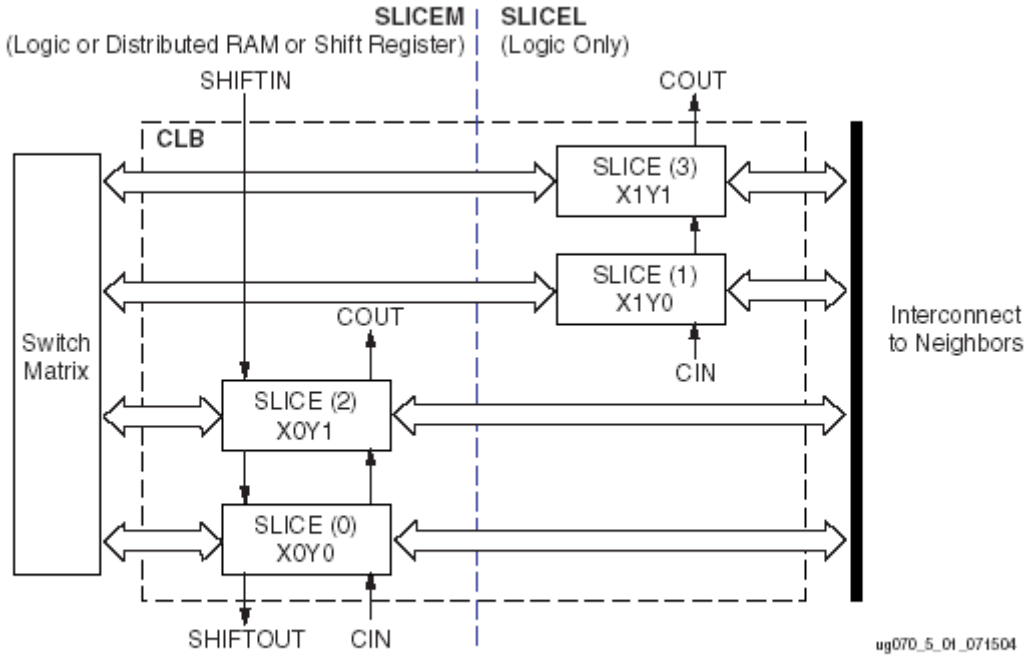


Figure 5-1: **Arrangement of Slices within the CLB**

Table 5-1: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	Distributed RAM	Shift Registers(1)
4	8	8	8	2	64 bits	64 bits

Notes:

1. SLICEM only

Altera Stratix II
Adaptive logic Module

Figure 2–5. High-Level Block Diagram of the Stratix II ALM

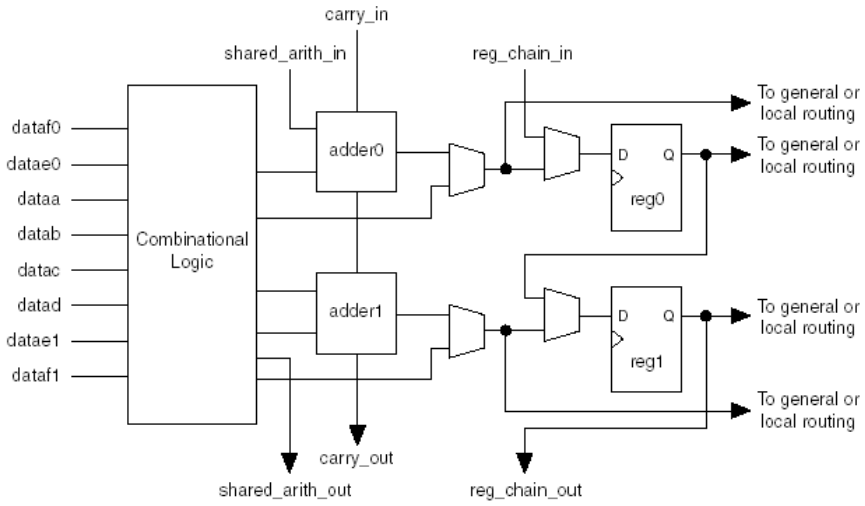
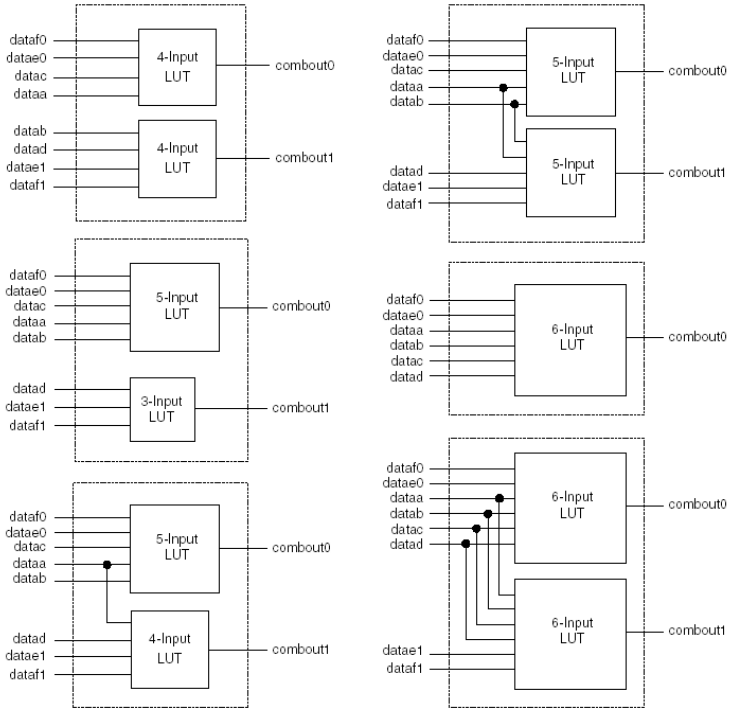


Figure 2–7. ALM in Normal Mode *Note (1)*



Note to Figure 2–7:
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

Podpora nových IO štandardov

Výrazná podpora pre Gigabitové prenosové rýchlosti

Altera Stratix II

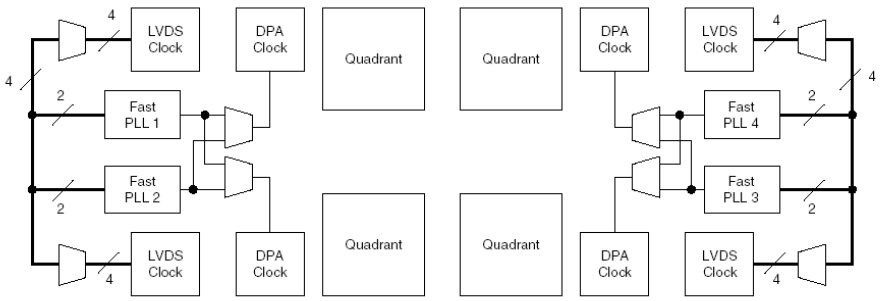
- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 156 channels with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM

Xilinx Virtex 4 *RocketIO™ MGT*

- 622 Mb/s to 10.3125 Gb/s data rates
- 8 to 24 transceivers per FPGA
- 3-tap transmitter pre-emphasis (pre-equalization)
- Receiver continuous time equalization
- Decision Feedback Equalizer (DFE) equalization for legacy backplane applications
- Optional on-chip AC coupled receiver
- Digital oversampled receiver for data rates up to 2.5 Gb/s
- Receiver signal detect and loss of signal indicator and out-of-band (OOB) signal receiver
- Transmit driver idle state for OOB signaling (both outputs at VCM)
- 8B/10B or 64B/66B encoding, or no data encoding (pass-through mode)
- Channel bonding
- Flexible Cyclic Redundancy Check (CRC) generation and checking
- Pins for transmitter and receiver termination voltage
- User reconfiguration using the Dynamic Configuration Bus
- Multiple loopback paths, including PMA RX-TX path

Príklad rozloženia PLL blokov pre vysielače a prijímače v Altera Stratix II

Figure 2–60. Fast PLL & Channel Layout in the EP2S15 & EP2S30 Devices *Note (1)*



Note to Figure 2–60:
(1) See Table 2–23 for the number of channels each device supports.

Podpora pre dešifrovanie konfiguračných dát, on-line dekompresia

Logika pre on-line dešifrovanie konfiguračných dát (použitý algoritmus **AES – Advanced Encryption Standard**, algoritmus nahradzuje starší DES) nemôže byť využitá na iné účely. Dešifračný kľúč pre AES je uložený v batériou zálohovanej RAM (Xilinx) alebo EEPOM (Altera) pamäti. Programovanie kľúča pomocou JTAG rozhrania.

Xilinx Virtex 4

Secure Chip AES bitstream encryption/decryption technology

Protect your intellectual property with security you can bank on. Virtex-4 FPGAs protect your design with AES (Advanced Encryption Standard) technology-the same technology used by financial institutions worldwide.

- Software-based bitstream encryption and on-chip bitstream decryption logic with dedicated memory for storing the 256-bit encryption key
- You generate the encryption key and encrypted bitstream using Xilinx ISE software. During configuration, the Virtex-4 device decrypts the incoming bitstream.

Battery-backed key provides unbreakable security

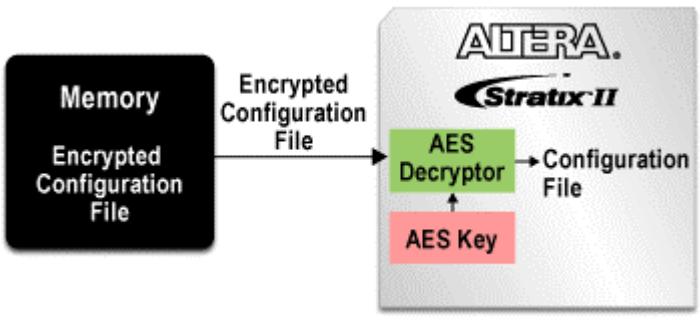
The Xilinx approach to security makes it virtually impossible for thieves to steal your design data. Virtex-4 FPGAs store the encryption key internally in dedicated RAM, backed up by a small externally connected battery (typical life 20+ years). It is not possible to read the encryption key out of the device. In contrast to protection schemes that use non-volatile key storage, any attempt to remove the Virtex-4 FPGA from the board in order to decapsulate the package for probing results in the instant loss of your encryption key and programming data.

Altera Stratix II

To provide designers with a means to protect their systems, Stratix II devices support configuration bitstream encryption using the advanced encryption standard (AES) and a 128-bit non-volatile key. Each Stratix II device can be securely configured with an encrypted configuration file generated by Quartus® II software and stored in an external configuration device. The Design Security web page has more information.

1. The 128-bit AES key is programmed into the non-volatile key storage in the Stratix II device.
2. The Quartus® II software uses the same AES key to generate an encrypted configuration file, which is then stored in a flash memory or configuration device.
3. At power-up, the flash memory or configuration device sends the encrypted configuration file to the Stratix II device, which then uses the stored AES key to decrypt the file and configure itself.

The encrypted configuration file cannot be decrypted without the key, preventing intellectual property theft.



AES Decryption in ProASIC3/E Devices

ProASIC3/E has a built-in 128-bit AES decryption core. The AES core in ProASIC3/E decrypts the encrypted programming file and performs a MAC check that authenticates the programming file prior to programming. This will ensure the following scenarios:

- Correct decryption of the encrypted programming file
- Prevention of erroneous or corrupted data being programmed during the programming file transfer
- Correct bitstream passed to the device for decryption

Figure 2 shows the use of AES in the ProASIC3/E devices.

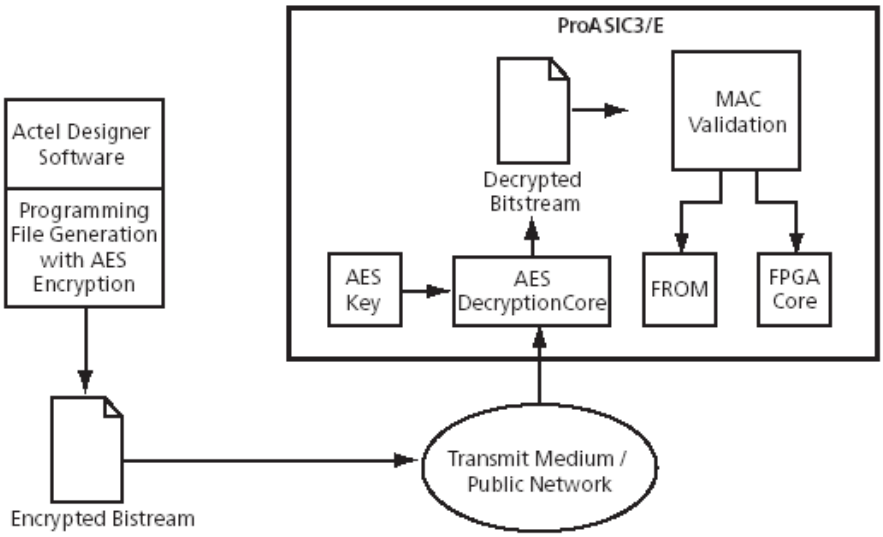


Figure 2 • **Example Application Scenario Using AES in ProASIC3/E Devices**