

### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 32 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Operating Voltage: 1.8 to 5.25 V

- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F500DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in one or two system clocks
- Up to 50 MIPS throughput

### Memory

- 64 kB Flash; in-system programmable; flexible security features
- 4352 bytes data RAM (256 + 4 kB)

### CAN 2.0B

- 32 message objects

### LIN 2.1

- Master or slave operation using dedicated hardware

### Digital Peripherals

- Up to 40 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with six capture/compare modules
- Four general-purpose 16-bit counter/timers
- External Memory Interface (EMIF)

### Clock Sources

- Internal programmable 0.5% oscillator: up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F500-IM, 48-Pin QFN (RoHS-compliant), 7 x 7 mm<sup>2</sup>
- C8051F500-IQ, 48-Pin QFP (RoHS-compliant), 9 x 9 mm<sup>2</sup>

